

VGA

640 X 480 LOW POWER MONOCHROME GREEN XL AMOLED MICRODISPLAY

DATASHEET *Revision C*

For Part Number:

Monochrome Green XL VGA Microdisplay (RoHS): EMA-100622-01

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| Revision Level | Date | ECN | Scope |
|----------------|------------|--------|---|
| 00 | 02-09-2015 | - | Initial Release |
| 01 | 09-10-2015 | | Update assembly drawing Update section 9.4.4 and 9.4.6 |
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1. INTRODUCTION

The VGA Monochrome Green XL RoHS device from eMagin Corporation is an active-matrix organic light emitting diode (AMOLED) microdisplay intended for near-to-eye applications that demand high image quality, compact size, and very low power. Combining a total of 1,060,800 active OLED dots, the VGA display is built on a single crystal silicon backplane and features eMagin's proprietary thin-film OLED XL technology offering extended life and luminance performance.

The active array is comprised of 680 x 520 square pixels with a 15-micron pitch and a 75% fill factor. An extra 40 columns and 40 rows (beyond the 640 x 480 main array) are provided to enable the active VGA display to be shifted by steps of 1 pixel in the X and Y directions for temporal dithering or optical alignment purposes. Additional dummy and test pixels surround the active array. Each full pixel is laid out as three 5 x 15 micron identical sub-pixels, which together form the 15-micron square triad group. Monochrome capability is accomplished by building the display without color filter, and configuring it for monochrome use. In this case, each pixel has a built-in triple redundancy (3 sub-pixels per pixel sharing the same information)

The VGA design features eMagin's proprietary "Deep Black" architecture that ensures off- pixels are truly black, automatically optimizes contrast under all conditions, and delivers improved pixel uniformity. Video data is received via an extended 10-bit digital interface with external synchronization and clocks, and the display includes on-chip digital to analog conversion, automatic luminance regulation over the full temperature range, automatic gamma correction, and programmable brightness. A dedicated monochrome mode allows the use of a single 10-bit input path in order to minimize power consumption.

The VGA display system provides broad versatility and flexibility for the user through application of a separate FPGA driver IC or integration of drive logic into the user's electronics using eMagin provided source code. The driver IC provides control over gamma, color balance, contrast, brightness, electronic optical alignment, and video formatting.

The VGA Monochrome Green XL microdisplay described in this datasheet is RoHS compliant.

In addition, the VGA display carrier board also includes a non-volatile memory component, accessible via the I2C serial bus. This component contains the preferred register settings for the VGA microdisplay.

Detailed device specifications and application information for the VGA XL microdisplay produced by eMagin Corporation are provided in this document.

2. GENERAL DESCRIPTION

Monochrome Green XL VGA Microdisplay

| Parameter | Specification ¹ |
|--|--|
| Display Type | Emissive, Monochrome Active Matrix Organic Light Emitting Diode on Silicon |
| Format | 640 (x3) x 480 pixels |
| Total Pixel Array | 680 (x3) x 520 pixels |
| Pixel Aspect Ratio | 15 micron square sub-pixel group |
| Pixel Arrangement | Three vertical sub-pixels |
| Display Area | 10.02 x 7.80 mm (12.84 mm diagonal, 0.50") |
| Useable Display Area | 9.6 x 7.2 mm (12.0 mm diagonal, 0.47") |
| Mechanical Envelope | 16.5 x 18 x 4.82mm (rigid carrier board) |
| Weight | ~ 2 grams |
| Gray Levels | 256 per pixel |
| Uniformity | > 90% end to end |
| Contrast Ratio | > 10,000:1 typical |
| Dimming Ratio | >400:1 with CR> 1,000:1 typical |
| White Luminance | ≥ 1500 cd/m ² (front luminance), VGA 60Hz VESA mode |
| Video Interface | 10-bit Digital 2.5V CMOS |
| Video Source Clock | 50 MHz maximum (VESA mode), up to 120 Hz frame rate |
| Control & Serial Interface | Digital 2.5V CMOS |
| Power Interface | |
| IO/Front-end Supply (VDD) | 2.5 Volts DC @ 5 mA maximum |
| Array/Analog Supply ² (VAN) | 5.0 Volts DC @ 25 mA maximum |
| Bias Supply (VPG) | -1.5 Volts DC @ 1 nA maximum |
| Operating Ambient Temperature | -46°C to +70°C |
| Storage Temperature | -55°C to +90°C |
| Humidity | 85%RH non-condensing |

Note 1: The above data represents performance specifications, measured at 20°C.

Note 2: Includes internally generated negative cathode supply.

3. FUNCTIONAL OVERVIEW

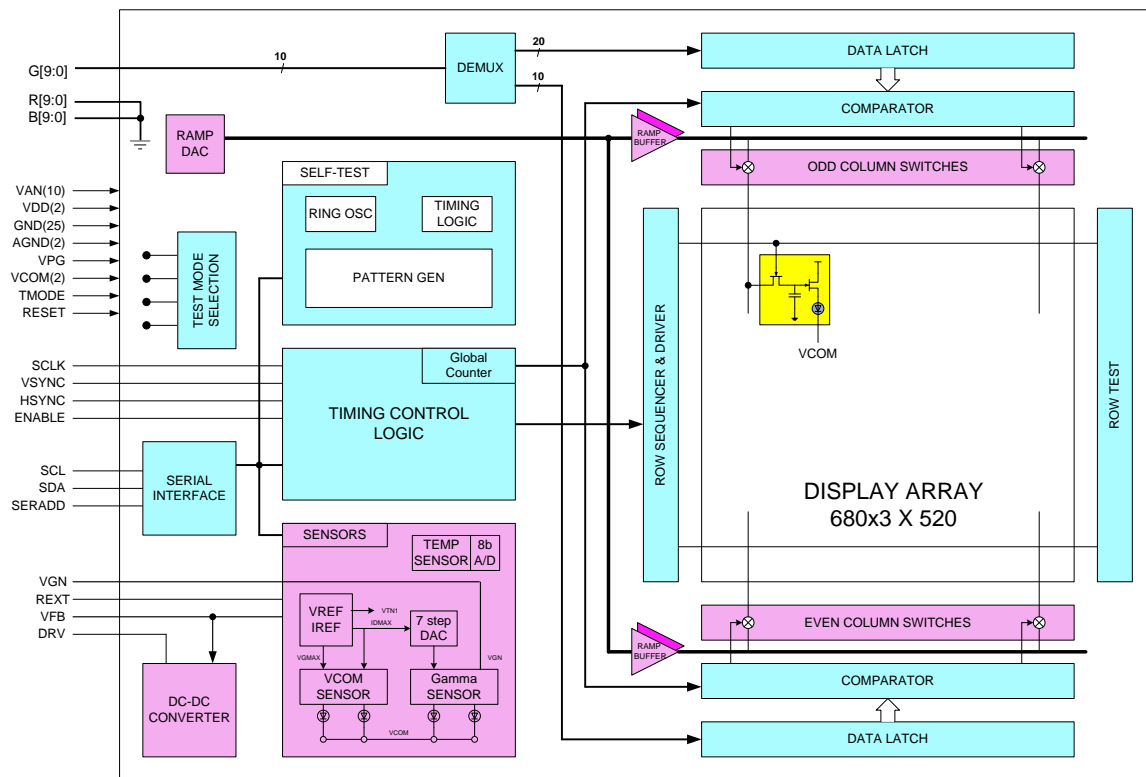


Figure 1 : Monochrome VGA design block diagram

The top-level block diagram for the VGA microdisplay is shown in Figure 1 and Figure 1. Bi-directional row and column sequencer circuits are used for addressing individual cells within the 680 x 520 x 3 pixel array, and internal digital-to-analog conversion circuits are included for converting the digital input data into the analog signals needed for programming the pixels. A storage element (capacitor) resides at each pixel cell that is used to set the gray level.

The digital video input data is applied individually to each of the three sub-pixels of the pixel. The data inputs that make up the digital data port are configured as three 10-bit data busses. Odd columns are driven by data sequencers located at the top of the array and even columns by bottom side sequencers. To obtain a linear gray-scale response from the OLED pixels the digital input data must be formatted with Gamma correction.

The IC backplane is designed for color and monochrome operation. In monochrome mode, a single 10-bit input port is used, and a single 10-bit data path is used internally to minimize power consumption. A demultiplexer switch applies the single data to the three columns that make up the pixel. The other two data channels are powered down.

The pixel clock and sync signals for various video formats are supplied externally and converted into individual control signals by the internal timing logic block.

Both progressive and interlaced modes are available and configured via the register-based interface.

The sensor block provides a number of signals for setting and regulating the display operation. These include a digital readout of the on-chip temperature, a reference level for maintaining constant luminance over temperature, a gamma correction feedback signal, and internal reference levels used for programming luminance over a wide range.

An on-chip dc-to-dc converter controller allows for the generation of the OLED cathode supply, relying on a few external passive components. The converter is an adjustable inverter that converts VAN to a negative supply used to bias the cathodes connected in common for all the array pixels via the VCOM input.

The 2-wire serial interface is a slave only I²C compatible controller with a programmable address via an external pin (LSB). The interface provides access (read and write) to on chip registers. The registers will allow the display to be configured for its various video modes and associated clock parameters. Additional control settings include luminance control, image orientation and position, internal vs. external function selection, self-test mode and various sensor settings.

The RESETB pin provides an asynchronous hardware reset function. When this pin is set to zero the display will turn off and the internal registers will be reset to their default state. After this pin is released (set to VDD), bit DISPOFF in register DISPMODE must be set high in order for the display to turn-on. If unused, this pin may be left unconnected.

The display also includes extensive functionality to support test and manufacturability including scantest for the logic blocks, row/column continuity test, JTAG pad continuity test, and a built-in test pattern generator.

Table 3-1 : VGA Microdisplay Video Formats

| Format (columns x rows) | Name | Input Mode | Output (Display) Mode |
|--------------------------------|-------------|-------------------|------------------------------|
| 640 x 480 Color / Mono | VGA | Progressive Scan | Progressive Scan |
| 640 x 480 Color / Mono | VGA | Interlaced Scan | Interlaced Scan |

4. INPUT / OUTPUT DESCRIPTION

Miniature 50 pin connector part number: DF12NB(3.0)-50DP-0.5V(51) or Hirose DF12D(3.0)-50DP-0.5V (Obsoleted by manufacturer as of 12/31/2021)

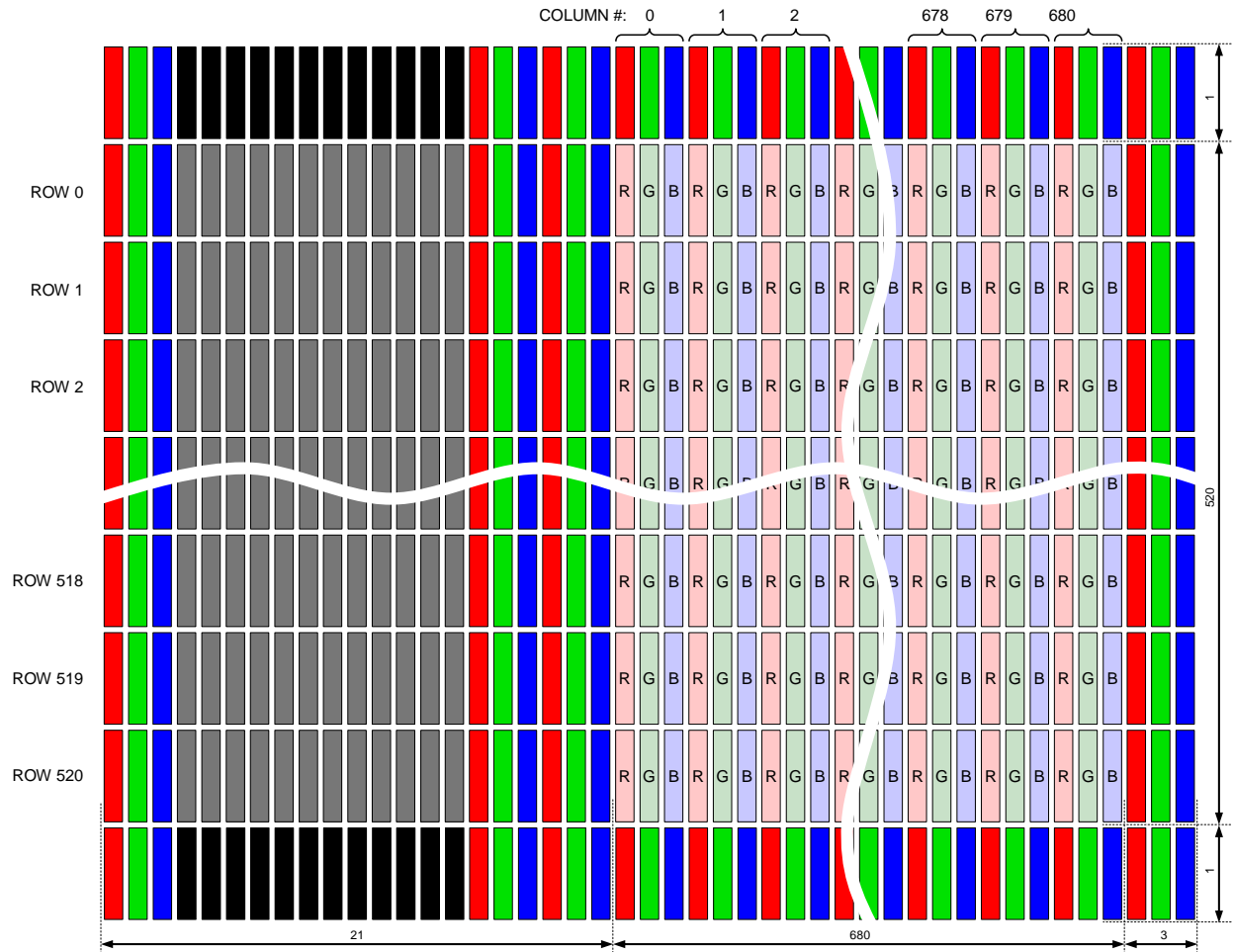
When driving Monochrome VGA displays, data should be applied to the Green input bus only. Red and Blue signals are not required and it is recommended that signals, RD0 to RD9 and BL0 to BL9, be connected to the ground signal at the source for the Monochrome displays.

Table 4-1: Input / Output Pin Description for Monochrome Green VGA Display

| Pin # | Pin Name | I/O | Signal Level | Description |
|-------|----------|--------|--------------|---|
| 1 | VDD2.5 | IN | Power | Logic and I/O power supply (2.5V) |
| 2 | VDD5 | IN | Power | Analog and Array power supply (5V) |
| 3 | SCL | IN | Digital | Clock port for the serial interface (400 KHz Max) (5V tolerant) |
| 4 | VDD5 | IN | Power | Analog and Array power supply (5V) |
| 5 | SDA | IN/OUT | Digital | Data port for the serial interface (5V tolerant) |
| 6 | GND | IN | Analog | External analog ramp input signal (0 to 5V range). Tie 20pF cap to GND when not in use. |
| 7 | SERADD | IN | Digital | Serial Interface LSB address bit. Must be connected. (2.5V CMOS) |
| 8 | GND | IN | Power | Power return terminal |
| 9 | RD0 | IN | Digital | Not active, connect to GND |
| 10 | VPG | IN | Power | Negative supply for array protection (-1.5V) |
| 11 | RD1 | IN | Digital | Not active, connect to GND |
| 12 | BI | IN | Digital | Burn In Mode selection pin. Active high. Internal pull-down. (2.5V CMOS) |
| 13 | RD2 | IN | Digital | Not active, connect to GND |
| 14 | VGN | OUT | Analog | Gamma sensor feedback signal (0 to 2.5V analog output) |
| 15 | RD3 | IN | Digital | Not active, connect to GND |
| 16 | GND | IN | Power | Power return terminal |
| 17 | RD4 | IN | Digital | Not active, connect to GND |
| 18 | VSYN | IN | Digital | Vertical Sync logic input. (2.5V CMOS, 1.8V Compatible) |
| 19 | RD5 | IN | Digital | Not active, connect to GND |
| 20 | HSYN | IN | Digital | Horizontal Sync logic input. (2.5V CMOS, 1.8V Compatible) |
| 21 | RD6 | IN | Digital | Not active, connect to GND |
| 22 | DE | IN | Digital | Data Enable logic input used with loading RGB data. (2.5V CMOS, 1.8V Compatible) |
| 23 | RD7 | IN | Digital | Not active, connect to GND |
| 24 | GND | IN | Power | Power return terminal |
| 25 | RD8 | IN | Digital | Not active, connect to GND |
| 26 | SCLK | IN | Digital | System clock input. (2.5V CMOS, 1.8V Compatible) |
| 27 | RD9 | IN | Digital | Not active, connect to GND |
| 28 | ENABLE | IN | Digital | Enable logic input. When inactive, blocks row and column sequencers. (2.5V CMOS, 1.8V Compatible) |
| 29 | GND | IN | Power | Power return terminal |
| 30 | RESETB | IN | Digital | Asynchronous System Reset. Active low. Internal pull-up. (2.5V CMOS, 1.8V Compatible) |
| 31 | BL0 | IN | Digital | Not active, connect to GND |
| 32 | GN9 | IN | Digital | Digital Green input (2.5V CMOS, 1.8V Compatible) |
| 33 | BL1 | IN | Digital | Not active, connect to GND |
| 34 | GN8 | IN | Digital | Digital Green input (2.5V CMOS, 1.8V Compatible) |
| 35 | BL2 | IN | Digital | Not active, connect to GND |
| 36 | GN7 | IN | Digital | Digital Green input (2.5V CMOS, 1.8V Compatible) |
| 37 | BL3 | IN | Digital | Not active, connect to GND |
| 38 | GN6 | IN | Digital | Digital Green input (2.5V CMOS, 1.8V Compatible) |
| 39 | BL4 | IN | Digital | Not active, connect to GND |
| 40 | GN5 | IN | Digital | Digital Green input (2.5V CMOS, 1.8V Compatible) |
| 41 | BL5 | IN | Digital | Not active, connect to GND |
| 42 | GN4 | IN | Digital | Digital Green input (2.5V CMOS, 1.8V Compatible) |
| 43 | BL6 | IN | Digital | Not active, connect to GND |
| 44 | GN3 | IN | Digital | Digital Green input (2.5V CMOS, 1.8V Compatible) |
| 45 | BL7 | IN | Digital | Not active, connect to GND |
| 46 | GN2 | IN | Digital | Digital Green input (2.5V CMOS, 1.8V Compatible) |
| 47 | BL8 | IN | Digital | Not active, connect to GND |
| 48 | GN1 | IN | Digital | Digital Green input (2.5V CMOS, 1.8V Compatible) |
| 49 | BL9 | IN | Digital | Not active, connect to GND |
| 50 | GN0 | IN | Digital | Digital Green input (2.5V CMOS, 1.8V Compatible) |

5. PIXEL ARRAY LAYOUT

Note: the figure below shows a color pixel array. For the monochrome green XL microdisplay, each R,G,B subpixel has the same color, defined by the Organic OLED stack.



6. ELECTRICAL CHARACTERISTICS

Table 6-1 : Absolute Maximum Ratings

| Symbol | Parameter | Min | Typ. | Max. | Unit |
|--------|---|------|------|---------|------|
| VDD | Front End Power Supply | -0.3 | | 2.75 | VDC |
| VAN | Array Power Supply | -0.3 | | 5.5 | VDC |
| VCOM | Common electrode bias | -6 | | 0 | VDC |
| VPG | Array Bias Supply | -3 | | 0 | VDC |
| VI | Input Voltage Range | -0.3 | | VDD+0.3 | VDC |
| VO | Output Voltage Range | -0.3 | | VDD+0.3 | VDC |
| PD | Power Dissipation | | | 1 | W |
| Tst | Storage Temperature | -55 | | +90 | °C |
| Tj | Junction Temperature | -45 | | +125 | °C |
| Ilu | Latch up current | | | +100 | mA |
| Vesd | Electrostatic Discharge – Human Body Model | | | ±2000 | V |

Stresses at or above those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the following tables is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability (except for the reverse bias condition. See below). Prolonged exposure to high temperatures will shorten the luminance half-life.

Table 6-2 : Recommended Operating Conditions

| Symbol | Parameter | Min | Typ. | Max. | Unit |
|-------------------------|--|-------|------|-------|------|
| VDD | Front End Power Supply | 2.375 | 2.5 | 2.625 | VDC |
| VAN | Array Power Supply | 4.75 | 5 | 5.25 | VDC |
| VCOM | Common electrode bias | -5 | -2.0 | 0 | VDC |
| VPG | Array Bias Supply | -3 | -1.5 | 0 | VDC |
| Tst | Storage Temperature | -55 | | +90 | °C |
| Ta | Ambient Operating Temp. | -45 | +25 | +70 | °C |
| Pdt_mono ⁽²⁾ | Power Consumption Monochrome White/Green Display | 51 | 60 | 70 | mW |

(1) & (2)

- Minimum power consumption is for an all pixels off display condition at room temperature
- Typical power consumption is for an all pixels on display condition at 80 cd/ at room temperature
- Maximum power consumption is for an all pixels on display condition at 200 cd/m2 at room temperature

Table 6-3 : DC Characteristics

(Ta = 25°C, VDD = +2.5V, VAN = +5V, GND = 0V)

| Symbol | Parameter | Min | Typ. | Max. | Unit |
|-------------------------|--|---------|------|---------|------|
| VDD | Front End Power Supply | | 2.5 | | V |
| VAN | Array Power Supply | | 5 | | V |
| VCOM | Common electrode bias | -5 | -2.0 | 0 | V |
| VPD | Array Bias Supply | | -1.5 | | V |
| Vil | Digital input low level | GND-0.3 | | 1 | V |
| Vih | Digital input high level | 1.8 | | VDD+0.3 | V |
| Vol | Digital output low level | | | 0.5 | V |
| Voh | Digital output high level | 2.4 | | | V |
| Vsl | Hsync, Vsync input low | GND-0.3 | | 1 | V |
| Vsh | Hsync, Vsync input high | 1.8 | | VDD+0.3 | V |
| VGN | Gamma feedback signal | 0 | | 2.5 | V |
| Ipix | Average Pixel Current per frame | 0 | 6 | 15 | nA |
| Ipix_dnl ⁽¹⁾ | Average Pixel Current Differential Non Linearity | | | 1 | % |

(1) Assumes a gamma corrected display with a nominal gamma of 1.0

Table 6-4 : AC Characteristics

(-45°C < Ta < +70°C, GND = 0V, VDD = +2.5V, VAN = +5.0V,
VCOM = -2V, VPG = -1.5V, I_{pix_avg} = 6 nA)

| Symbol | Parameter | Min | Typ. | Max. | Unit |
|----------|--|--------|----------|------|---------------------|
| SCLK | Video Clock Frequency | 12 | - | 50 | MHz |
| CLK_Duty | SCLK duty cycle | 40 | | 60 | % |
| Fhs | Horizontal Sync frequency | 15.734 | | 80 | KHz |
| Fvs | Vertical Sync Frequency | 30 | | 120 | Hz |
| Tlo | Line Overscan (% of line time) | 3 | | | % |
| Tfb | Frame Blanking (% of frame time) | 1 | | | % |
| Trst | Reset Pulse Width | 100 | | - | μs |
| Cin | Digital Pins Input Capacitance | | 3 | | pF |
| Cvpg | Pin VPG Input Capacitance | | 13.6 | | nF |
| Pd VAN | Average Van Power Consumption (VGA Mode 60 Hz refresh rate) | | 88 55 | | mW color mW mono |
| Pd VDD | Average VDD Power Consumption (VGA Mode 60 Hz refresh rate) | | 8 5 | | mW color mW mono |
| Pd VPG | Average VPG Power Consumption | | | 1 | mW |
| Pd PDWN | Total Power Consumption in PDWN (sleep) mode* | | 2.5 | | mW |
| Ta | Ambient Operating Temperature | -45 | | +70 | °C |

*Note: Input data, sync and clock lines must be inactive and held low

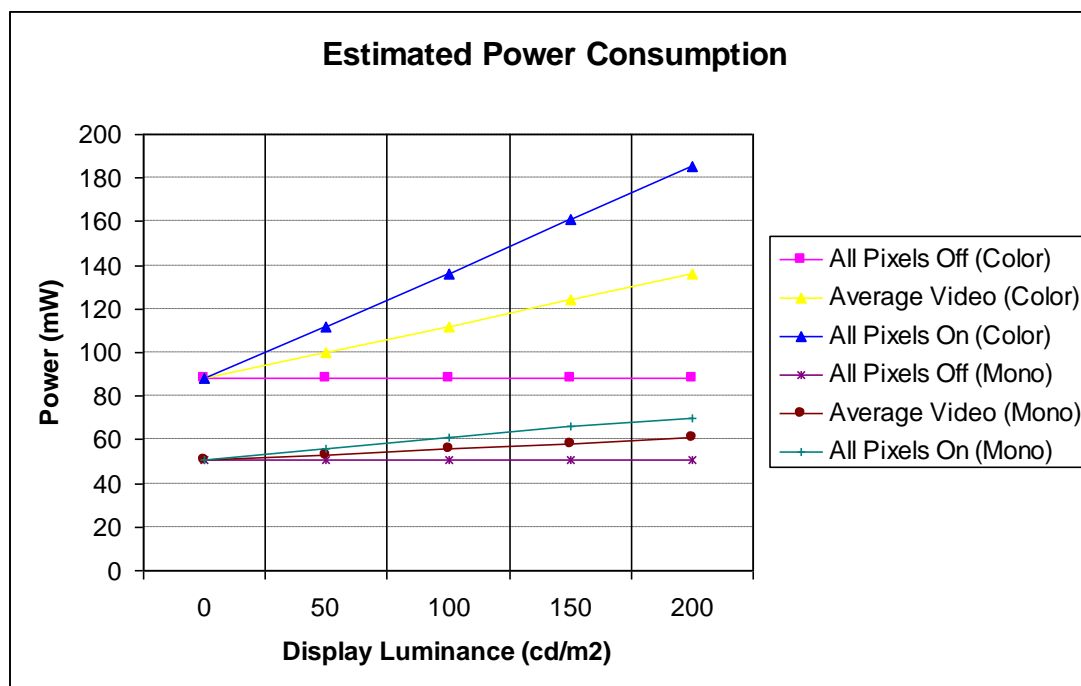


Figure 2 : Total estimated power consumption vs. luminance at 20°C

6.1 Timing Characteristics

6.1.1 Interface Timing Diagrams

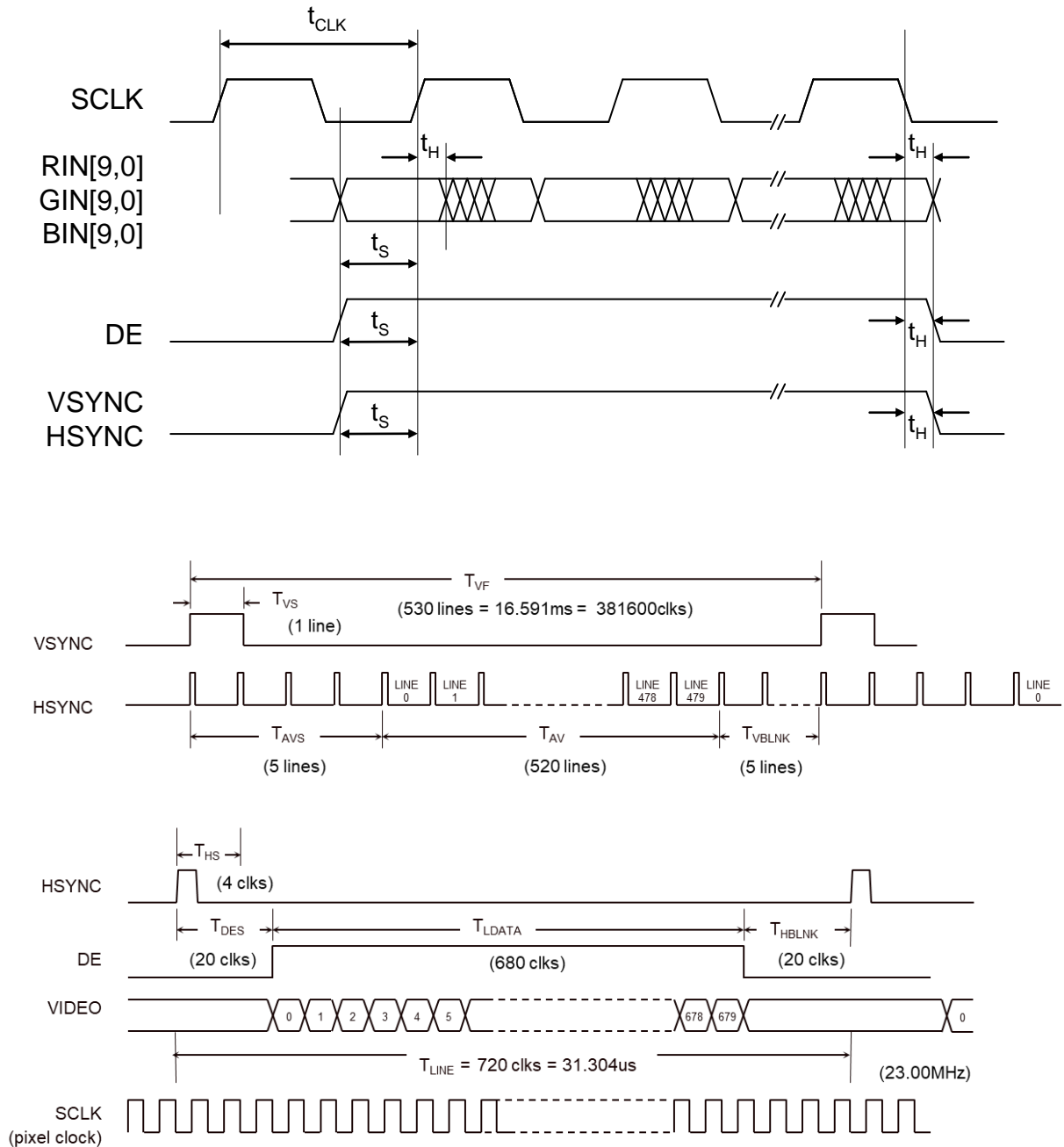


Table 6-5 : Input Timing Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|-----------|------|---------------------|------|--------------|
| Video Input Setup/Hold (RIN/GIN/BIN) | t_s | 4 | | | ns |
| | t_H | 1 | | | ns |
| Control Signals Setup/Hold (DE/HSYNC/VSYNC) | t_s | 4 | | | ns |
| | t_H | 1 | | | ns |
| Clock Frequency | f_{CLK} | | 25.175 ¹ | | MHz |
| Clock Period | t_{CLK} | | 39.72 | | ns |
| Clock Duty | D_{CLK} | 45 | | 55 | % |
| VSYNC Pulse Width | t_{VS} | 1 | | | Hsync period |
| Time to Active Video Start | t_{AVS} | 4 | | | Hsync period |
| Frame Blanking (% of frame time) | t_{FB} | 1 | | | % |
| HSYNC Pulse Width | t_{HS} | 4 | | | SCLK period |
| Time to DE Start | t_{DES} | 12 | | | SCLK period |
| Line Overscan (% of line time) | t_{LO} | 3 | | | % |

Note 1: VGA @ 60Hz frame rate

6.1.2 Gamma Sensor Timing Diagram

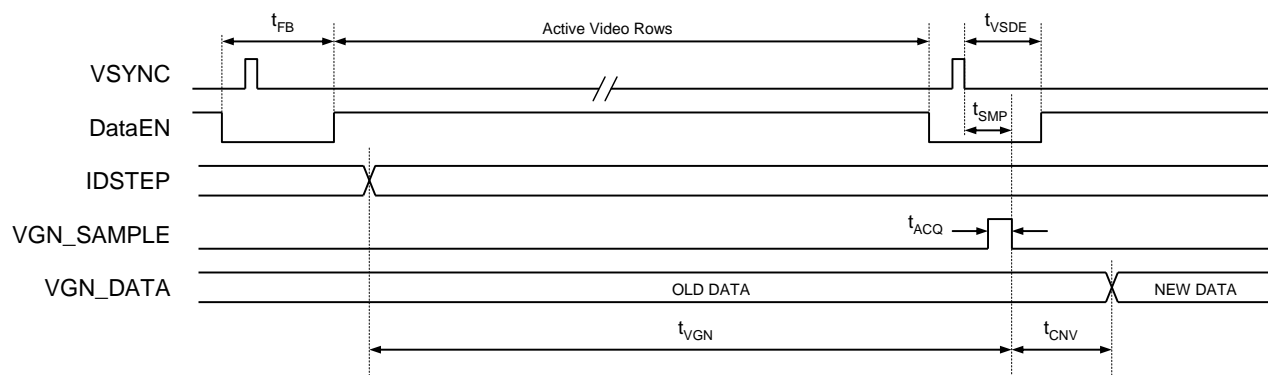


Table 6-6 : Gamma Sensor Timing Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------------------|-----------|-----------|------|------------|---------|
| IDSTEP to VGN Settling Time | t_{VGN} | 10 | | | ms |
| Frame Blanking (% of Frame Time) | t_{FB} | 1 | | | % |
| VGN Sampling Time | t_{SMP} | t_{ACQ} | | t_{VSDE} | |
| A/D Acquisition Time | t_{ACQ} | 20 | | | μs |
| A/D Conversion Time | t_{CNV} | | | | |

7. OPTICAL CHARACTERISTICS

Table 7-1: VGA XL Monochrome Green XL Microdisplay Optical Characteristics

Conditions: Ta = +20°C, VDD = +2.5V, VAN = +5V, VPG = -1.5V, VCOM = internally generated

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|--|---------------------|------|------|-------------------|
| LMAX | Front Luminance @ max gray level over dimming range (IDRF, DIMCTL) | 0.03 ⁽¹⁾ | 1500 | 3000 | cd/m ² |
| CR | White to Black Contrast Ratio | 1,000:1 | | | |
| CIE Green | CIE-X | 0.18 | 0.20 | 0.32 | |
| | CIE-Y | 0.50 | 0.59 | 0.67 | |
| GL | Gray Levels Per Color | 256 | | 1024 | levels |
| F _R | Refresh Rate | 30 | | 120 | Hz |
| FF | Emissive Area/Total Sub-pixel Area | | 0.69 | | |
| U _{LA} | End to end large-area uniformity | 85 ⁽²⁾ | | | % |
| S _{VH} | Pixel spatial noise at ½ luminance (1STD) ⁽³⁾ | | | 5 | % |
| S _{LOT} | Peak-to-peak luminance variation over operating temperature range ⁽⁴⁾ | | | 8 | % |
| T _{ON} | Time to recognizable image after application of power | | | 0.5 | sec |

Note 1: Minimum dimming level obtained when using the ROWRESET (05h) function.

Note 2: At 100% of gray level brightness and 1,000 cd/m² luminance. Luminance uniformity measured between the nominal values of five 1000 pixel zones located in the four extreme corners and the center zone of the display.

Note 3: Using a dedicated test pattern and measured at an equivalent flat field luminance of 55 foot-Lamberts (characterization data only, not a production test)

Note 4: With firmware providing temperature control of VDACMX setting

8. MECHANICAL CHARACTERISTICS

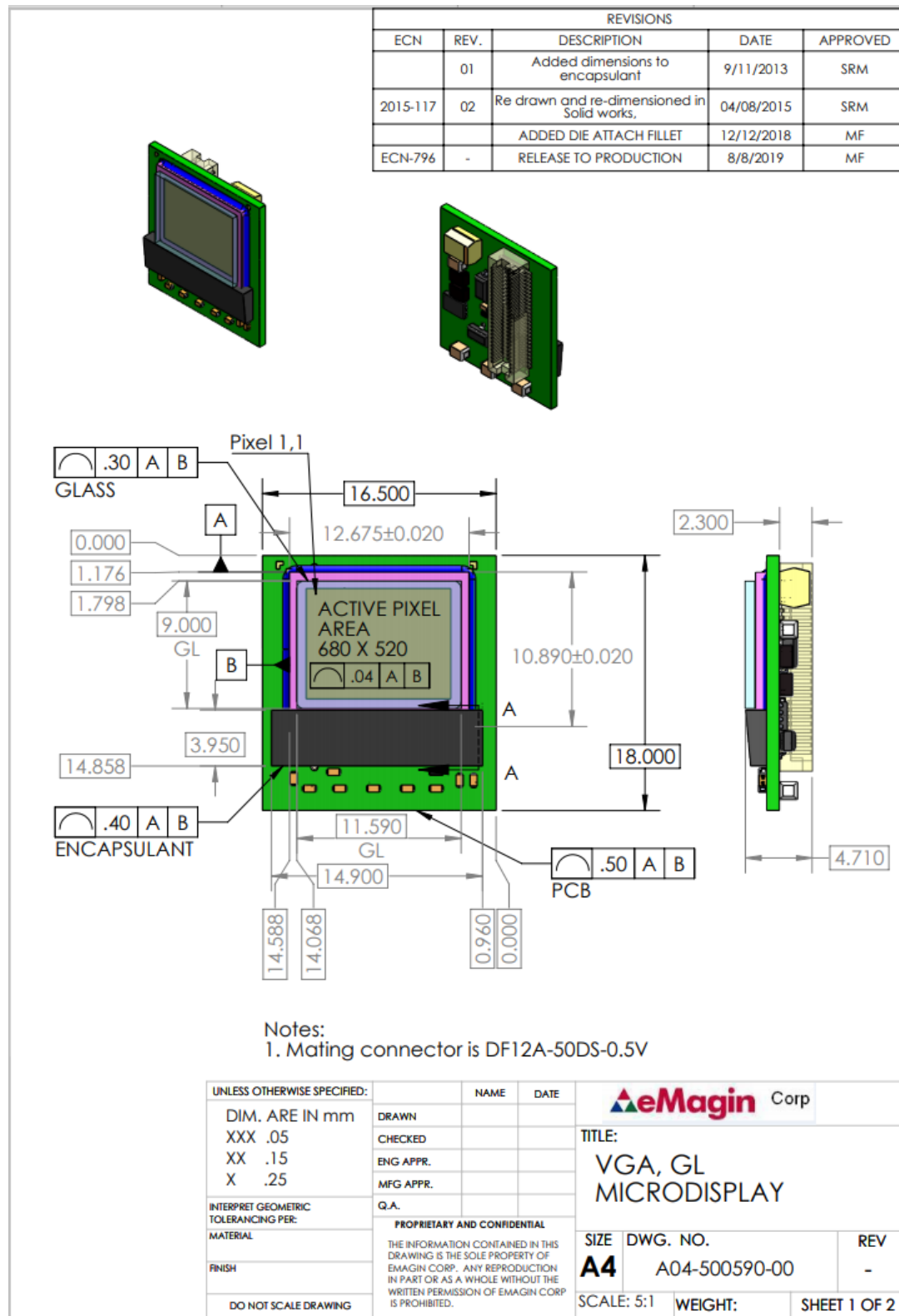
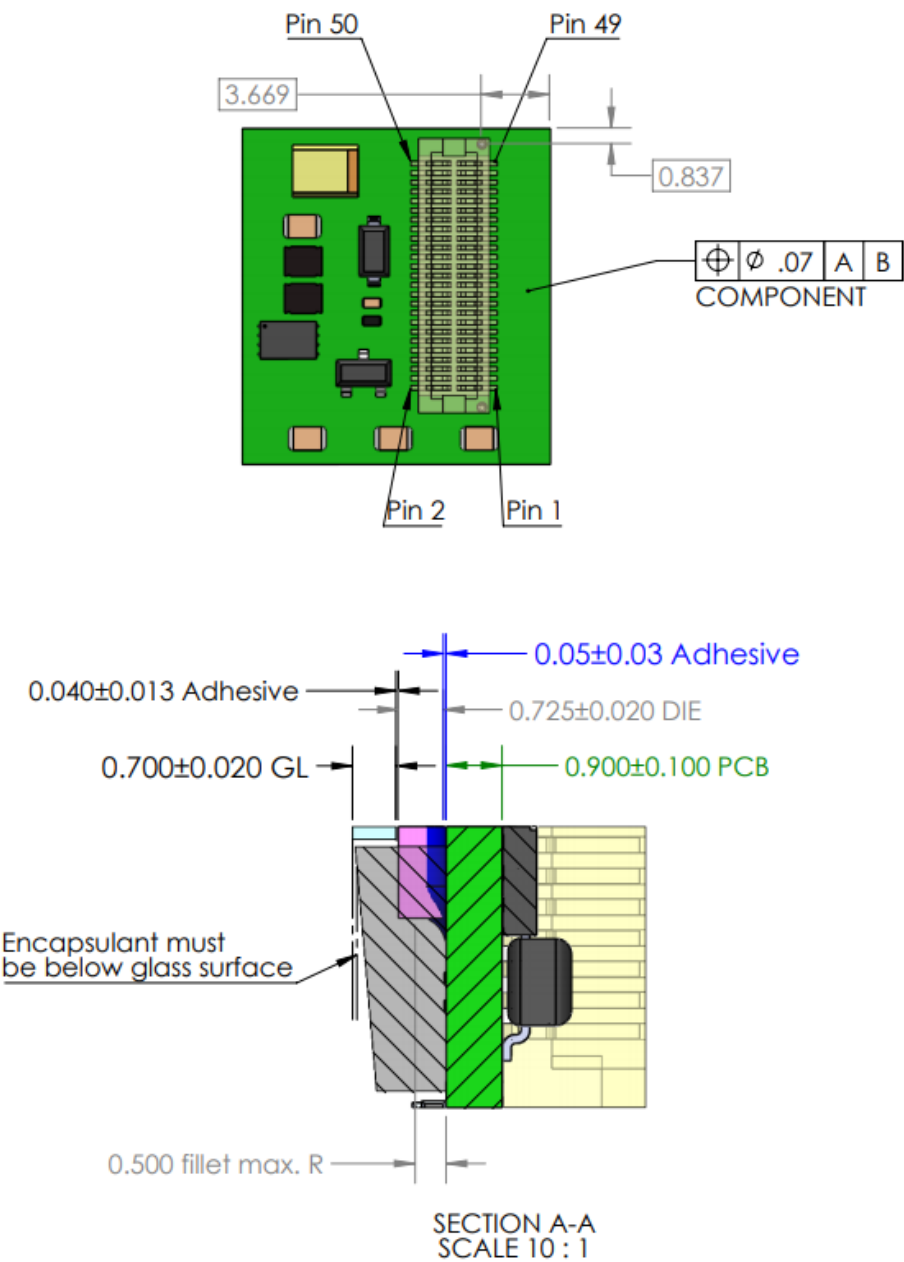



Figure 3: Monochrome VGA Microdisplay IC Drawing with 0.7mm Glass Cover



| | | | | | | | |
|---|--|---|--|--|--|---|--|
| UNLESS OTHERWISE SPECIFIED: | | NAME | | DATE | |  | |
| DIM. ARE IN mm | | DRAWN | | TITLE: VGA, GL MICRODISPLAY | | | |
| XXX .05 | | CHECKED | | | | | |
| XX .15 | | ENG APPR. | | | | | |
| X .25 | | MFG APPR. | | | | | |
| INTERPRET GEOMETRIC TOLERANCING PER: | | Q.A. | | SIZE DWG. NO. REV A4 A04-500590-00 - | | | |
| MATERIAL | | PROPRIETARY AND CONFIDENTIAL | | | | | |
| FINISH | | THE INFORMATION CONTAINED IN THIS DRAWING IS THE SOLE PROPERTY OF EMAGIN CORP. ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION OF EMAGIN CORP IS PROHIBITED. | | | | | |
| DO NOT SCALE DRAWING | | | | SCALE: 5:1 | | WEIGHT: SHEET 2 OF 2 | |

8.1 Color/Monochrome VGA Configurations

Connectors J1

Manufacturer: Hirose
Manufacturer Part Number: DF12NB(3.0)-50DP-0.5V(51)

Mating Connector Information

Manufacturer: Hirose
Manufacturer Part Number: DF12NC(3.0)-50DS-0.5V(51)

Weight: < 3 grams
Printed Circuit Board Material: FR4
Printed Circuit Board Tolerances: ± 0.25 mm (both axes)

Note

DF12D(3.0)-50DP-0.5V has been obsoleted by the manufacturer.

The replacement connector implementation started in January 2022.

The replacement connector color is black, and is form/fit/function compatible with the older part number.



Older version



Current version

9. DETAILED FUNCTIONAL DESCRIPTION

9.1 Video Input Interface

The 30-bit digital input port is comprised of three 10-bit data busses that make up the 3 subpixel data inputs. Separate synchronization signals (VSYNC and HSYNC) and the pixel clock (SCLK) are to be provided by the external video source. The data valid signal (DE) is used to signal the start of loading a row of data into the internal line memory. An active ENABLE signal is required for the Stereovision mode (inactive for all other modes, except Interlaced Video). The timing diagram for the input data bus is shown in Figure 4.

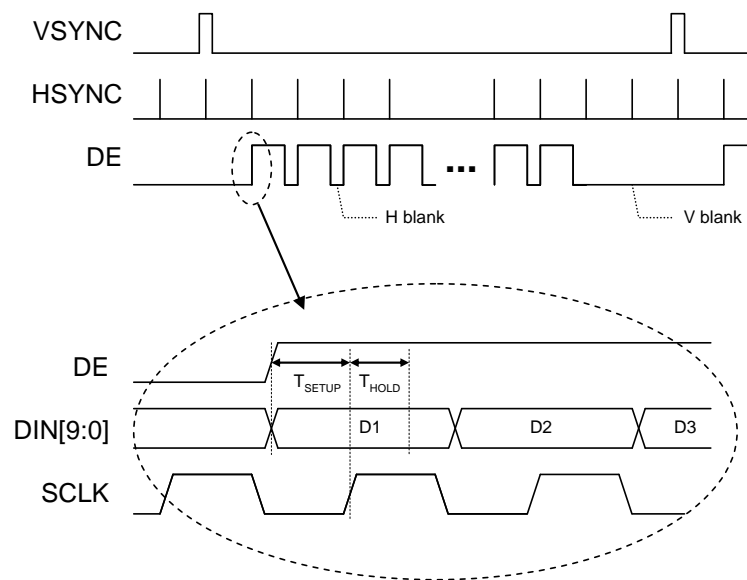


Figure 4 : Input Data timing diagram.

The input data to the display requires certain formatting that must be applied by the external drive electronics as described below.

9.1.1 Gamma Correction

Due to the non-linear electro-optic characteristic of the OLED pixel, a gamma correction signal must be applied to the video input signal to achieve a linear system response for the display. Since the optimum gamma curve will vary with temperature and luminance, it should also be regularly updated to account for changes in operating conditions. The typical OLED response to input data is a highly nonlinear characteristic. The Gamma Correction function shown in Figure 5 is obtained by inverting the OLED response function. The overall system display response becomes linear when the source video data is modified by the Gamma Correction function before being applied to the VGA.

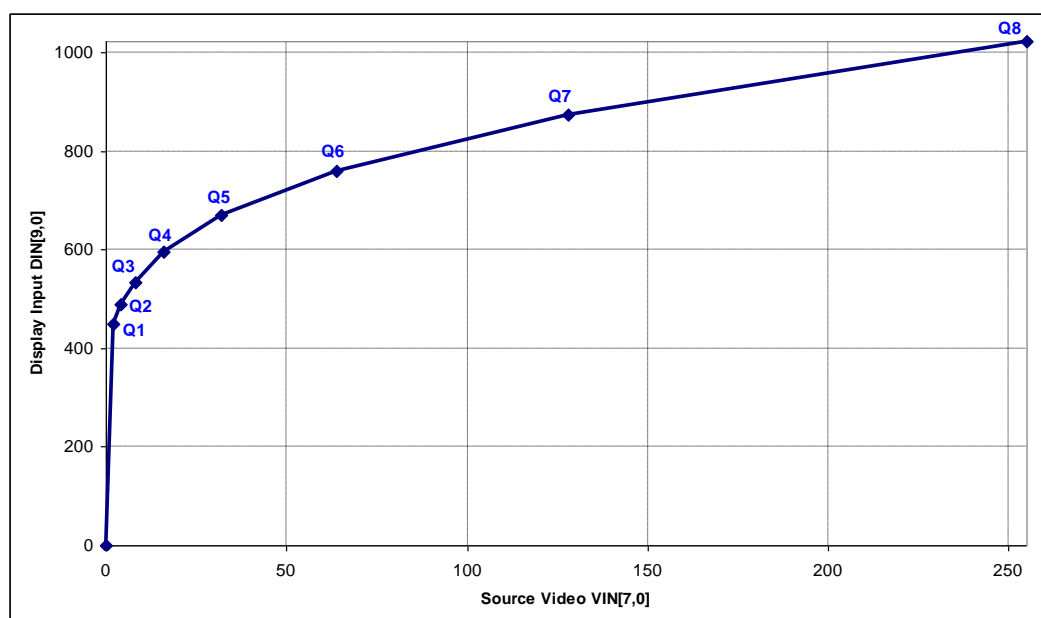


Figure 5: Typical VGA input transfer function

As shown in Figure 6, a typical VGA application will include a 256x10-bit look-up-table for each data channel located in the data path between the video source and the display. For the monochrome green VGA, only one data channel is used (referred to as the Green Channel). The LUT, which is contained in an external FPGA, converts the 8-bit data byte for each color of the video source into a 10-bit output data word for driving the microdisplay. The LUT is programmed with the gamma correction function required to linearize the system for the current operating conditions. Due to the non-linear characteristic of the OLED display, a 10-bit input to the VGA is used to ensure a linear 8-bit optical response with better than 1-lsb accuracy.

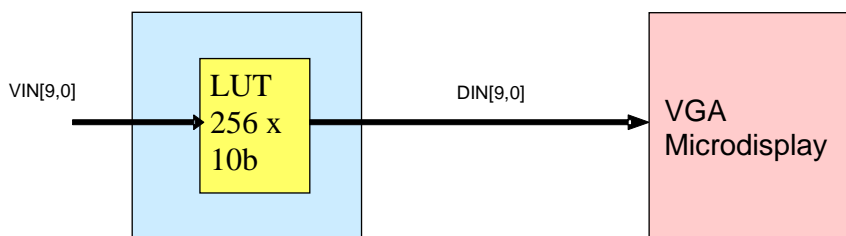


Figure 6: Gamma correction using a look-up table (LUT)

On-chip support for generating the gamma correction function in the form of an 8-segment piecewise-linear function is described in section 9.4.6. A total of 8 data points (Q1...Q8) that lie on the gamma curve as shown in Figure 5 are provided by the display chip. The external microcontroller can use this information to generate intermediate data points for the entire 256 point curve by linear interpolation.

9.1.2 Row Data Expansion

Since the display is comprised of 680 column lines, the external drive electronics should add 40 dummy pixels with black data to each row of 640 pixels provided by the source signal. The dummy pixels can be distributed between the start and end of the row data according to the desired horizontal location of the active window within the pixel array.

9.2 D/A Conversion

In this design the conversion of the video input signal into an analog drive signal at the pixel is carried out in a two-step process during each horizontal clock period. The digital input video data is first transformed into a precise time delay based on counts of the global RAMP clock. Second, the time delay triggers the column switch to sample the voltage of a linear ramp and to store the analog value on the column line capacitor. The selected pixel circuit copies the analog data and uses it for driving the OLED diode until it is refreshed during the next frame period.

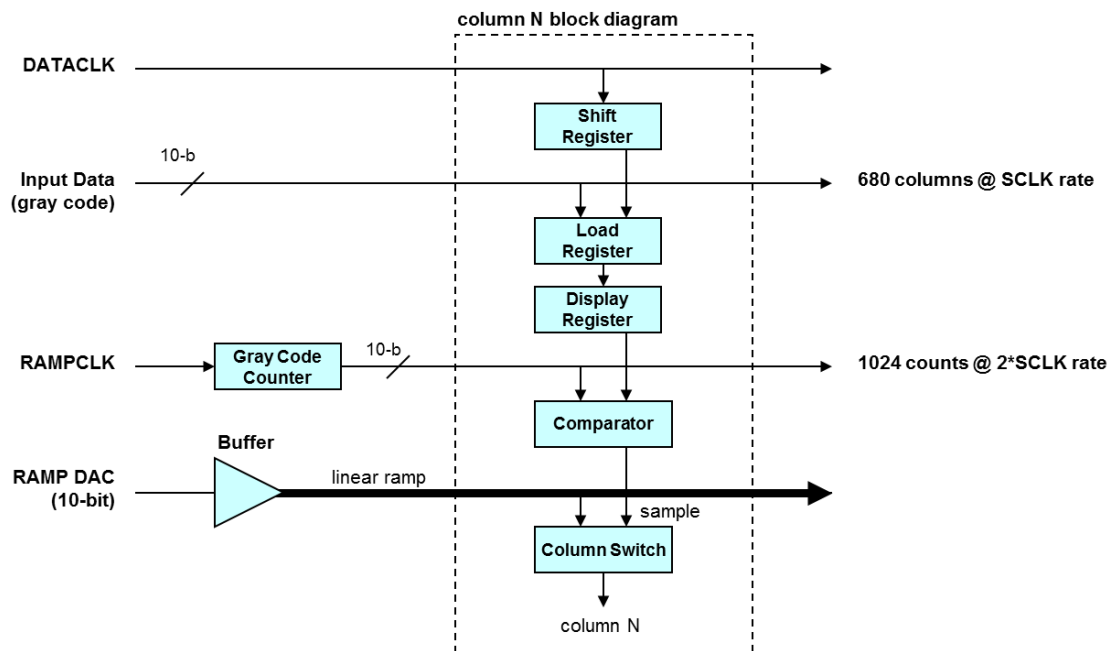


Figure 7 : Data sampling for Column N

A block diagram of one column drive circuit is shown in Figure 7. The 680 Display registers form a line memory that facilitates a pipeline mode of operation in which video data is converted to analog form and sampled by the pixels in row M during the same line period that video data for row M+1 is loading into the LOAD registers. At the end of each line period the data in the LOAD registers is transferred in parallel into the DISPLAY line memory. The externally supplied SCLK clock is used for both loading input data into the chip and for advancing the global column counter. There is a maximum latency of 2 line periods before data is displayed.

A timing diagram for the data sampling process is shown in Figure 8. The internal Ramp Generator operates at the HSYNC frequency and outputs a linear ramp with a slow rise-time and a fast reset capability that is buffered and applied to all the pixel array columns simultaneously. The RAMP signal starts synchronously with HSYNC (after a delay) with a positive slope from a zero voltage level and rises to a voltage near the VAN rail after 480 SCLK clock cycles as determined by a 10-bit counter. The start position of the RAMP can be adjusted via bit RAMPDLY in register RAMPCTL, its peak value can be set using register VDACMX, and the duration of the flyback transition can be selected between two options by the FLYBTIME bit in register RAMPCTL.

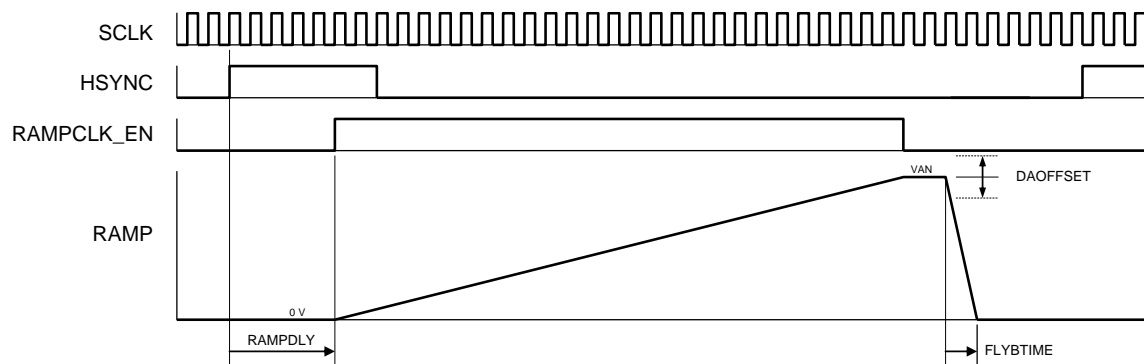


Figure 8 : Timing diagram for column data sampling

9.3 Format and Timing Control

Various control signals for the horizontal and vertical sequencers that are needed to implement the specified video formats are generated in the Timing & Control Logic block. The specific timing parameters are set by registers VINMODE, DISPMODE, TOPPOS, and BOTPOS using the serial interface.

The display starts up with the array in the off-state (black) by default and requires a command to the DISPOFF register bit via the serial interface to turn the display on. This provides the user with an opportunity to change the default startup conditions before the display lights up.

Bi-directional scanning is supported in both orientations via the DISPMODE register. Bit VSCAN sets the vertical scan direction, and bit HSCAN sets the horizontal scan direction.

Selection among the main supported display formats is done via register bits TOPPOS, BOTPOS, and the external drive electronics. The starting row is determined by register TOPPOS and the ending row by register BOTPOS, which are set by default so the active window in VGA mode is vertically centered in the array. These registers allow the active window to be shifted vertically in 1 pixel steps by up to 40 pixels.

The starting column is determined by the external drive electronics which must add 20 dummy black pixels to each row of incoming data as described previously. This allows the active window to be horizontally shifted in 1 pixel steps by up to 40 pixels total.

9.3.1 Interlaced Mode

Bit SCMODE in the DISPMODE register is used to select either progressive or interlaced mode for all formats. By default (SCMODE=0) the normal progressive mode is active. The interlaced mode is limited to a maximum of 512 and a minimum of 240 active rows per field.

Field status in interlaced mode is provided via the ENABLE input pin. The state of this pin is latched on the falling edge of VSYNC. When register bit SET_FIELD = “0” then a logic low at the ENABLE pin indicates that Field 1 (odd field) is active, and a logic high indicates that Field 2 (even field) is active. The opposite states are indicated when SET_FIELD is set to 1.

9.3.2 Stereovision

The VGA is designed with binocular stereovision applications in mind. As a result of the fast OLED response time and the presence of a storage capacitor at each pixel, the microdisplay can operate at low refresh rates without showing flicker.

This will allow the displays to be used with a frame or field sequential (more generally known as time sequential) stereovision mode using a single video input channel, and therefore providing a simple means to leverage the capabilities of PC compatible computers using stereo compatible graphics adapters, such as the NVidia GeForce series. The frame sequential stereovision mode supported should follow the Video Electronics Standards Association (VESA) Connector and Signal Standards for Stereoscopic Display Hardware. This standard is available from VESA at www.vesa.org.

The ENABLE input pin will allow for a direct implementation of the VESA standard without additional external components. The microdisplay can be programmed for either an active high or low Enable, allowing a single signal to be used with two displays. In such a configuration, one display scans and displays while the other one holds and displays.

The ENABLE input acts, when set low, as a mask for HSYNC and VSYNC. It does not blank the display but prevents it from acquiring another frame of data until released. This is a real time input. The active state (high or low logic level) is programmed by the SET_ENABLE bit in the VINMODE register.

The 3D-MODE bit of the DISPMODE register will be used to set either the Stereovision mode of operation (1) or Normal (non-3D) operation (0).

Frame Sequential Mode:

In Time Sequential Mode each video frame contains information for either the left or right eye. When 3D-MODE="1" the SCMODE bit in the DISPMODE register is set to Progressive Scan Mode (00H) for frame sequential mode. The following description for Frame Sequential operation assumes the source is in compliance with the VESA standard mentioned above, where the data for the left eye is provided while the Enable signal is at the logic high level, and the data for the right eye display is provided while the Enable signal is at the logic low level. The stereovision mode is controlled by both the Enable input pin and by the SET_ENABLE bit of the VINMODE register. The Enable input signal is sampled into the circuit by a flip-flop clocked on the falling edge of VSYNC and the sampled value will be used for the next frame. (The Enable signal is generated by the graphics software and may not be synchronized to the VSYNC signal).

To activate the stereovision mode, the right eye display needs to be configured with Enable active low (SET_ENABLE= "0"). This will allow the right eye microdisplay to hold the previous frame while the Enable input is high. The left eye display must be configured with Enable active high (SET_ENABLE="1"). Thus the two Enable inputs can be tied together to the incoming Stereo Sync signal provided by the graphics adapter (or other custom source). This is illustrated by the timing diagram shown in Figure 9: Timing for frame sequential stereovision mode.

Line Interleaved Mode:

In Line Interleaved Mode each video frame contains information for both the left and right eyes. Consequently, the resolution is reduced in half for each display but they both run at the full frame rate. The operation of the Enable input pin and the SET_ENABLE bit will be similar to Frame Sequential Mode except that now the Enable input toggles at the line rate.

For standard VGA operation, the SET_ENABLE bit needs to be set to 0 (logic low), which is the power-on default value, and the Enable pin input needs to be tied to Ground.

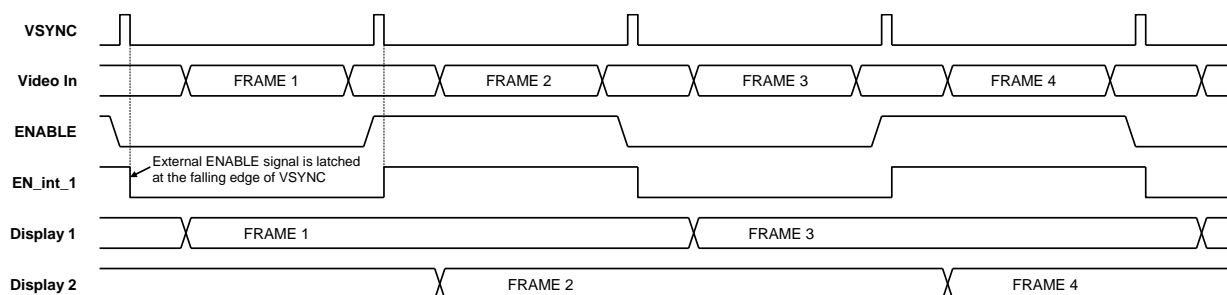


Figure 9: Timing for frame sequential stereovision mode

9.4 Sensor Functions

9.4.1 Temperature Readout

An on-chip temperature sensor provides continuous device temperature information via the serial interface. The sensing circuitry allows for calibration at power-up via dedicated registers, TREFDIV[5,0] and TEMPOFF[7,0]. The temperature reading is digitized on-chip and stored in a dedicated register, TEMPOUT[7,0]. A register bit, TSENPDP in register ANGPWRDN, is able to power down the sensor.

The temperature sampling period is controlled by register TUPDATE[7,0] which allows the temperature reading to be updated between every 50msec to 4.25sec when operating at a 60Hz frame rate.

9.4.2 Luminance Regulation Sensor

Register VGMAX[7,0] controls the pixel drive voltage used for regulating the maximum luminance value. By default this level is set to about 4.95V when the VAN supply is equal to 5V to avoid saturating the video buffers. It can be adjusted over a range of 4 to 5V.

Register VDACMX[7,0] is used to set the maximum value of the internal Ramp DAC generator. This value should match the internal VGMAX setting for best luminance accuracy and control. The optimum setting can be derived by measuring luminance for different values of VDACMX as described in 11.9.

9.4.3 Pixel Bias Sensor

Register BIASN[1,0] sets a bias current for the OLED array in order to achieve improved control of black level and color saturation at the expense of a small increase in power consumption. In the default setting (BIASN=1) the bias contributes to a 10mW increase of power consumption for the array. It is recommended to use the BIASN=1 setting for best performance.

9.4.4 Luminance Control (Analog Dimming)

A variable luminance level is achieved by controlling the maximum pixel current while maintaining the largest possible dynamic range. Dimming control for the display is effected by adjusting the 7-bit register DIMCTL via the serial interface to provide 128 linear steps in brightness ranging from near zero to the maximum level set by register IDRFB. This functionality is only available for VCOMMODE=0 or 1.

The bits IDRFB_COARSE in register IDRFB provide a coarse adjustment of the maximum luminance level, while the IDRFB_FINE bits enable the coarse level to be fine-tuned. Figure 10 shows the typical luminance levels in a color display for various settings of the IDRFB register when DIMCTL is set for maximum brightness.

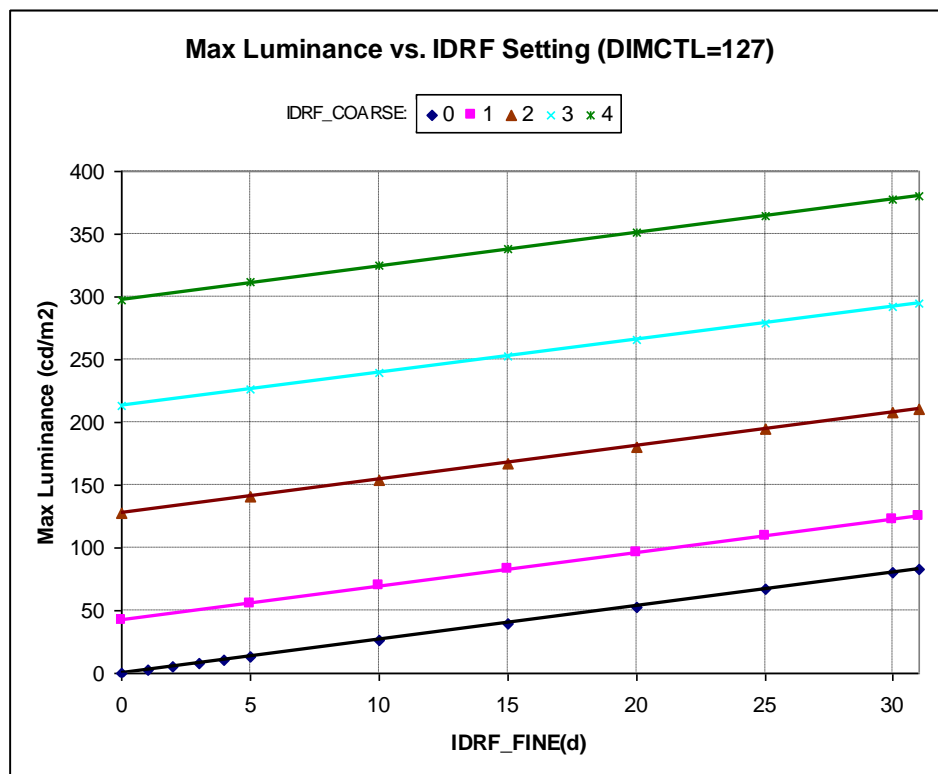


Figure 10: Typical maximum luminance for various IDRF settings

9.4.5 Luminance Control (PWM Dimming)

A variable luminance level can also be achieved by setting the frame on-time of the video image using register ROWRESET (05h). This register controls the fraction of a frame period during which the input video data is displayed (on-time). The display is set to black for the off-time or non-display portion of the frame period as shown in Figure 11.

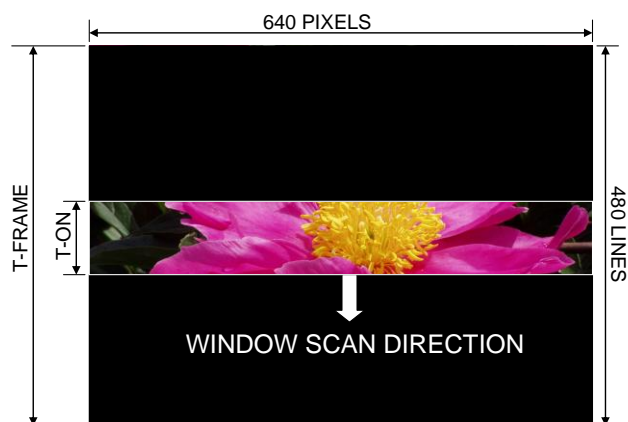


Figure 11: Video display during PWM dimming control

PWM dimming via ROWRESET can be used in combination with the analog dimming function to achieve an extended luminance control range since both modes operate independently. For any luminance level achieved via the IDRF and DIMCTL settings, the ROWRESET function will enable the luminance to be varied over a range of 0.4 to 100%.

9.4.6 Gamma Correction Sensor

The gamma sensor is provided as an aid to generating a linear optical response from the VGA display system. As described previously, an external 256-entry look-up-table is required to transform input video data into a gamma-corrected data signal for driving the microdisplay input port. The VGA display generates an internal real-time representation of the gamma correction curve for the current operating conditions. This representation is in the form of an analog voltage waveform which can be sampled one point at a time at the VGN pin for eight specific values on the curve. A specific value VGN_i , corresponding to one of 8 internally fixed grayscale levels GL_i , is selected by setting bit IDSTEP in register GAMMASET via the serial port. Eight sequential measurements are required to complete the gamma table. The gamma table can then be used to reconstruct an approximation of the ideal gamma correction curve using piece-wise linear interpolation, or by employing a curve fitting algorithm to achieve more accuracy if desired. This function is only available for VCOMMODE=00h.

An external A/D converter is required to convert each VGN measurement into digitized form and to store the values in a microcontroller for further processing. A full frame period following a change in the IDSTEP bit should be provided to allow the VGN signal to settle before sampling it to 10-bit precision by the external A/D converter. It is recommended to sample the VGN signal during the frame blanking interval for best results.

The VGN readings are normalized and converted to a 10-bit full-scale word $DVGN_i[9,0]$ using the following expression:

$$DVGN_i[9,0] = \frac{VGN_i}{VGN_{MAX}} * 1023$$

Each of these data values must be further multiplied by a correction factor CF_i to obtain the Gamma table coefficients as follows:

$$GC_i[9,0] = DVGN_i * CF_i$$

NOTE

The GC_i factors are determined at factory test for each display and written to the on-board eeprom for retrieval by the host firmware starting at address 60h and ending at address 72h, with two bytes allocated for each GC value (see EEPROM map in Appendix D).

Typical values for factor CF_i are given in Table 9-1 and Table 9.2. The CF values are determined at the factory for the VGA product.

Table 9-1: Correction Factor values for VGA CFXL with a150 cd/m² luminance

| CF1 | CF2 | CF3 | CF4 | CF5 | CF6 | CF7 | CF8 |
|-------|-------|-------|-------|-------|-------|-------|-----|
| 0.875 | 0.890 | 0.905 | 0.922 | 0.940 | 0.955 | 0.968 | 1 |

Table 9-2 Correction Factor Values for VGA MGXL with a 190 cd/m² peak luminance

| CF1 | CF2 | CF3 | CF4 | CF5 | CF6 | CF7 | CF8 |
|-------|-------|-------|-------|-------|-------|-------|-----|
| 0.850 | 0.890 | 0.902 | 0.918 | 0.925 | 0.940 | 0.960 | 1 |

Using the derived values for GC_i and their corresponding grayscale coordinates GL_i , the 8-entry Gamma Correction table consisting of data points $Q_i = (GL_i, GC_i)$ can be constructed. The outcome of a typical gamma sensor measurement and calculation procedure is shown in Table 9-3.

Table 9-3: Sample Gamma Correction Table

| i | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---------------|-------|-------|-------|-------|-------|-------|-------|-------|
| $IDSTEP[0]$ | 0h | 1h | 2h | 3h | 4h | 5h | 6h | 7h |
| $VGN_i(volt)$ | 1.839 | 1.876 | 1.913 | 1.964 | 2.045 | 2.159 | 2.318 | 2.500 |
| $GC_i(dec)$ | 662 | 698 | 727 | 766 | 814 | 872 | 941 | 1023 |
| $GL_i(dec)$ | 2 | 4 | 8 | 16 | 32 | 64 | 128 | 255 |

The full 256-word LUT is derived from the Gamma Coefficient Table using linear interpolation to generate intermediate data points as illustrated in Figure 12. The input to the LUT for each data channel of the video source is represented by the 8-bit signal VIN[7,0], and the output of the LUT (which is also the input to the microdisplay) is represented by the 10-bit signal DIN[9,0]. For example, the Y coordinate for the intermediate point Q(x, y) on the line segment formed between the gamma table points Q6 and Q7 is obtained by:

$$Y = Y_6 + (Y_7 - Y_6) * \frac{(X - X_6)}{(X_7 - X_6)}$$

The intermediate points for other line segments are found in similar fashion. A software routine in the system microcontroller is used to perform the necessary calculations. The software is also used to convert the LUT data into Gray Code format before loading it into the data-path LUTs in the FPGA. A buffer LUT should be used in the FPGA to temporarily store the data as it is transferred from the microcontroller

via the serial port. When the buffer LUT is full, the data can be rapidly transferred to the data-path LUTs during a frame blanking time to avoid disturbing the displayed image.

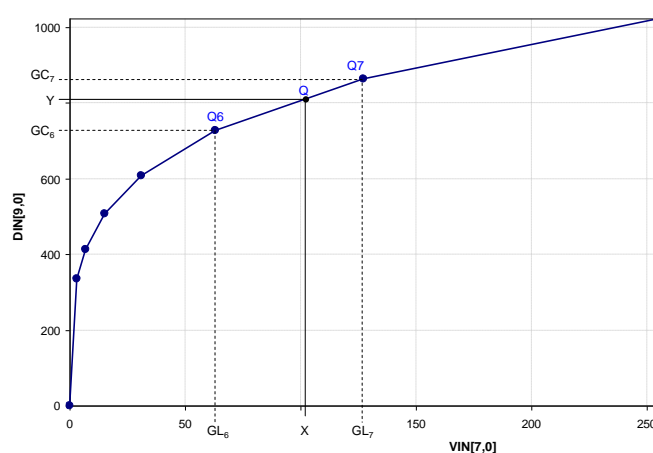


Figure 12: Gamma curve generated using PWL function

A smooth transition of the gamma curve at the lowest gray levels is essential for best performance of the display at the black end of the gray scale. Refer to Figure 14 for an illustration of the recommended approach for calculating the gamma curve at low gray levels. The LUT data points for gray levels 1 to 4 can all be generated by linear extrapolation from the gamma points Q1 and Q2. The LUT data point for gray level 0 (also defined as Q0) is a fixed value that is user-defined, and normally should be set to a very low value, e.g. 1, to ensure the best black level. The value for Q0 is shown on the graphical interface screen supplied with the VGA design reference kit for user convenience. It is not affected by the gamma sensor signal and can only be changed manually by user input.

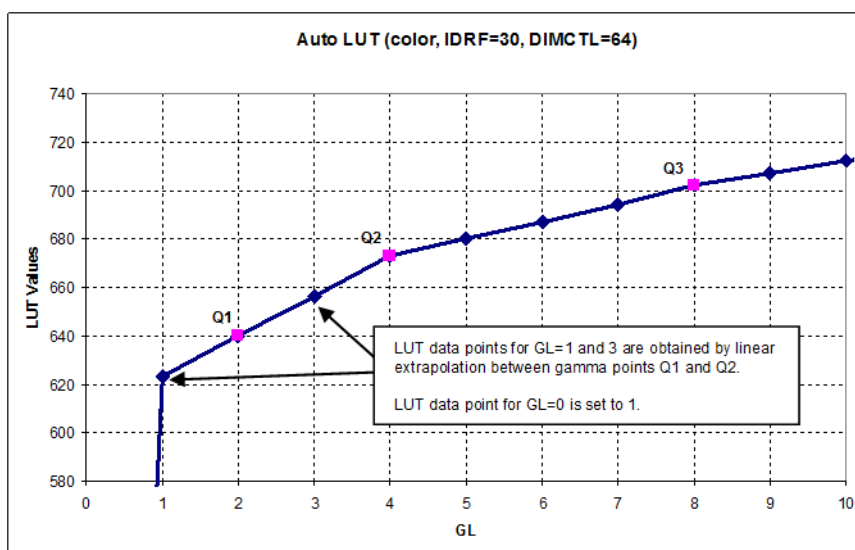


Figure 13: Gamma curve at low gray levels

An arbitrary optical response function for the microdisplay can be obtained by performing an additional operation on the gamma coefficients before generating the gamma correction curve as described previously. For example, the relationship between the output luminance of the display (y) and the gray level input to the LUT (x) can be defined in terms of the system gamma (γ) by the following expression:

$$y = x^\gamma$$

The corresponding gamma coefficients are then given by the following expression:

$$GC_i^\gamma = \left(\frac{VGN_i}{VGN_{MAX}} * CF_i \right)^\gamma * 1023$$

For the case of a linear optical response ($\gamma=1$) this expression reduces to the simpler form given previously. Examples of gamma curves generated from the same VGN values for different settings of the System Gamma parameter are shown in Figure 15 and the corresponding system response curves for the display are given in Figure 16.

The System Gamma function is implemented in the VGA DRK Firmware and is accessible to the user in the DRK UI Software.

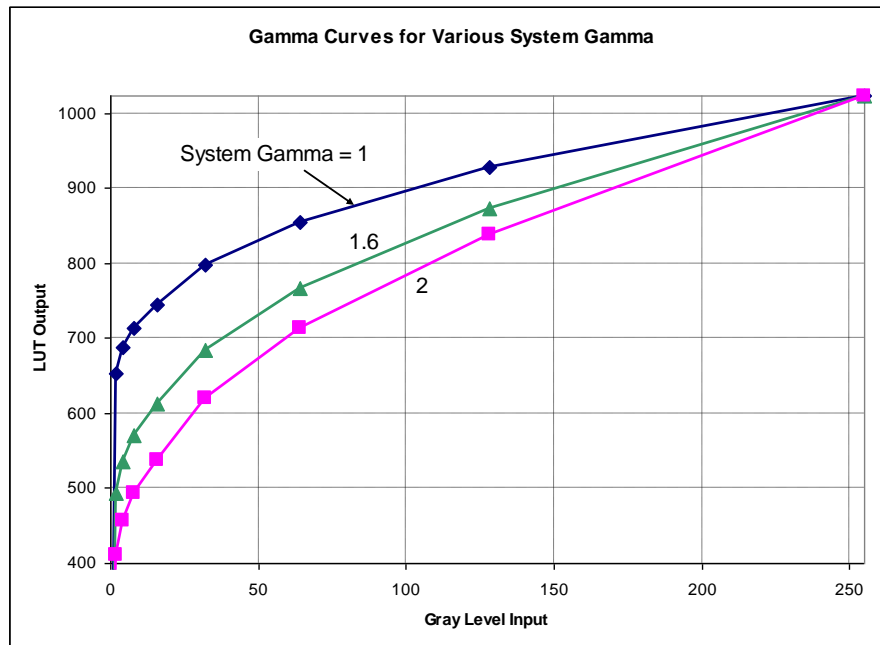


Figure 14 : Gamma curves for arbitrary System Gamma

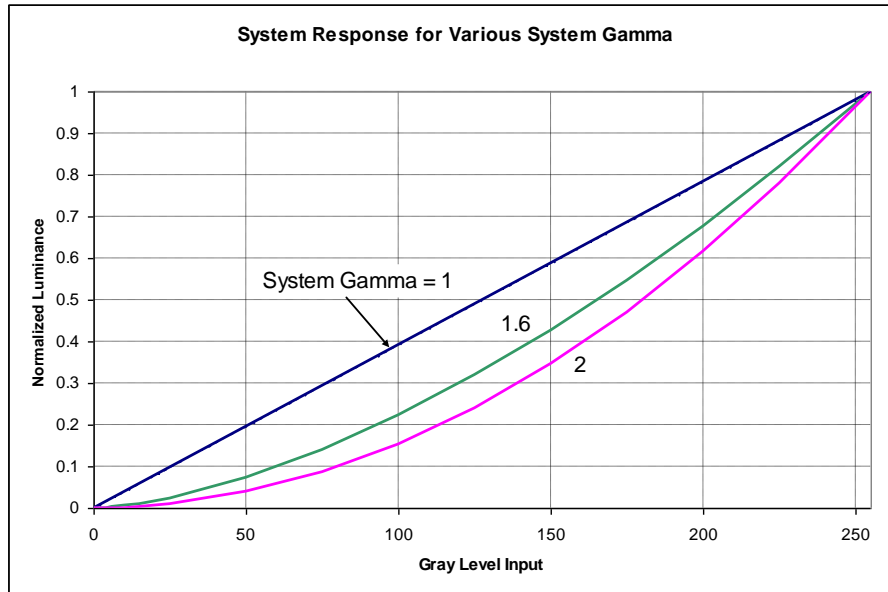


Figure 15 : Display system response for arbitrary system gamma

9.5 DC-DC Converter

An on-chip dc to dc converter controller allows for the generation of the OLED cathode supply, relying on a few external passive components assembled on the display carrier board. The converter is an adjustable inverter that converts VAN to a negative supply used to bias the OLED via the VCOM input pin. Adjustment is managed by the control logic and registers VCOM[7,0] and VCOMMODE[1,0].

The converter adjustment comes from two sources:

- A nominal value set in a dedicated register that provides for the room temperature voltage level.
- The output of an internal VCOM sensor circuit. This feature can be enabled/disabled via register setting to allow full external control (via register VCOM).

A soft-start function is provided that allows the converter output to ramp up in a controlled fashion by sensing the switch current and limiting its peak value.

A block level schematic of the Cuk converter that is employed in the VGA application is shown in Figure 16.

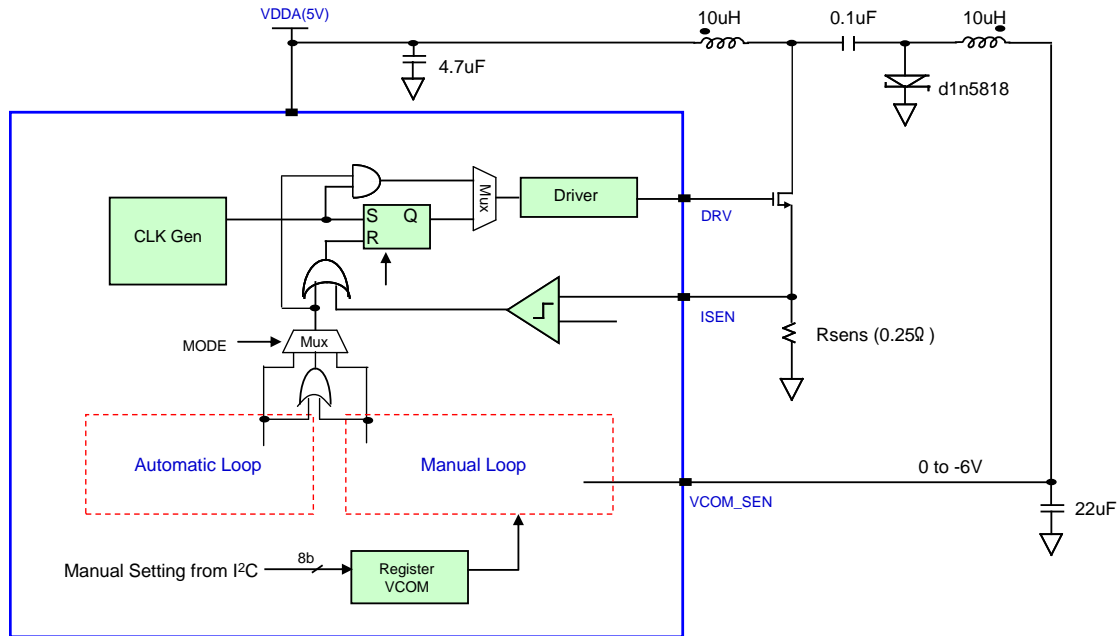


Figure 16 : Schematic of DC-DC controller function

Three modes of operation, selected via register VCOMMODE, are provided for the controller function. Mode 1, selected by default (VCOMMODE=0), activates the Automatic Loop which provides VCOM regulation based on an internal current feedback sensor. In this mode the cathode supply is automatically regulated in order to maintain a constant maximum OLED array current over changes in temperature and luminance. The cathode voltage will tend to rise in absolute value as the luminance level is increased or the operating temperature is reduced.

Mode 2, selected by setting VCOMMODE=1h, is a hybrid control mode that prevents the absolute value of the cathode supply from becoming too small at higher temperatures, but allows it to increase at low temperatures where it is needed to ensure a stable regulated OLED current. Both the AUTO and MANUAL control loops are running simultaneously in this mode with one taking charge above a user defined threshold (set by register VCOM) and the other below that threshold. For relatively low temperatures and high luminance levels the AUTO mode will be in control and the cathode supply will follow the trajectory shown in Figure 17. If operating conditions try to force the absolute value of the cathode supply to drop below the threshold, then the control switches to MANUAL mode and the regulated supply remains fixed at the VCOM level.

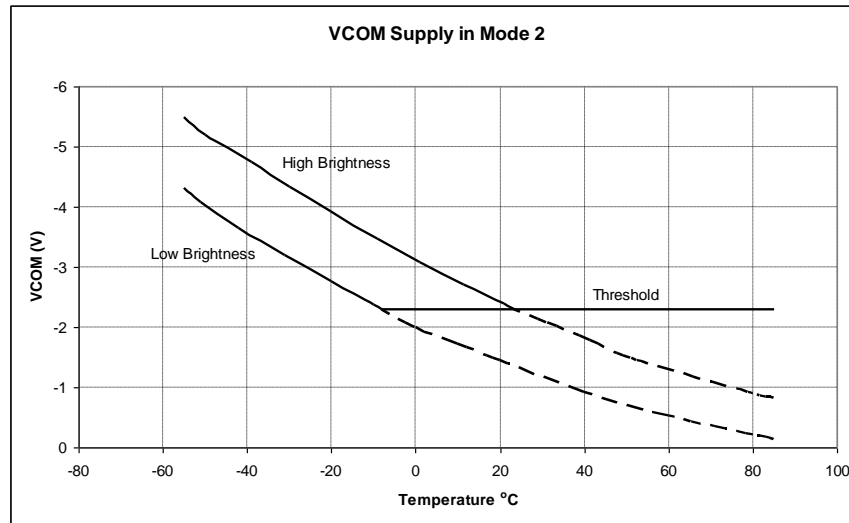


Figure 17 : VCOM supply characteristic in Mode 2

Mode 3, selected by setting VCOMMODE=2h, activates the Manual Loop which provides a fixed cathode supply based on a cathode voltage feedback signal. The actual value of the cathode voltage is controlled over a range of 0 to -6V by setting register VCOM. Its default value is about -2.3V. In this mode the dimming and luminance regulation functions via IDRFB and DIMCTL are not operational. Luminance is controlled directly via the VCOM register setting in this mode instead.

9.6 I²C Serial Interface

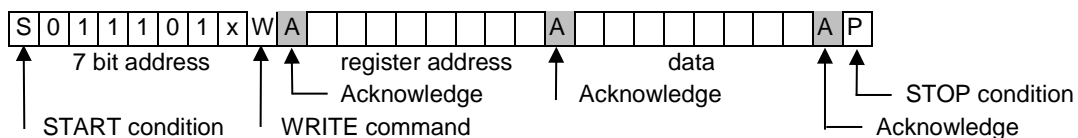
The serial interface consists of a serial controller and registers. The serial controller follows the I²C protocol. An internal address decoder transfers the content of the data into appropriate registers. The protocol will follow the address byte followed by register address data byte and register data byte sequence (3 bytes for each register access):

Serial address with write command
Register address
Register data

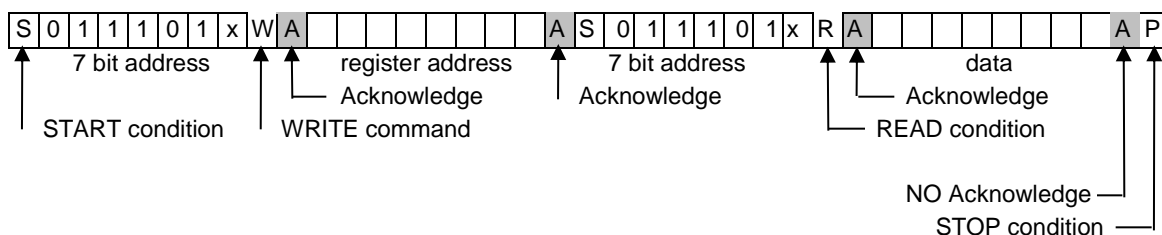
The registers are designed to be read/write. Read mode is accomplished via a 4 byte sequence:

Serial address with write command
Register address
Serial address with read command
Register data

RANDOM REGISTER WRITE PROCEDURE



RANDOM REGISTER READ PROCEDURE



The serial controller is capable of slave mode only.

The x in the 7-bit address code is set by the SERADD input pin and is provided to allow a dual display and single controller configuration.

Slave Address: 011101X where X = 0 or 1 depending on the status of the SERADD pin. This is summarized in Table 9-3.

Write Mode: Address is 74h (or 76h if SERADD = 1)

Read Mode: Address is 75h (or 77h is SERADD =1)

Sequential Read/Write Operation:

The serial controller allows for both sequential and read operational modes. For either mode, the host needs only set the initial register address followed by as many data bytes as needed, taking care not to issue a STOP condition until all desired data bytes have been transmitted (or received).

Maximum interface frequency: 400 KHz.

Table 9-4 : I²C Address Summary

| VGA | | 0 | 1 | 1 | 1 | 0 | 1 | SA | w/r |
|------|-------|---|---|---|---|---|---|----|-----|
| SA=0 | write | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| | read | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| SA=1 | write | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| | read | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

9.7 Power-On Sequence

To ensure proper startup and stabilization of the display the following power-on sequence is recommended:

1. Turn on VDD, VAN, and VPG supplies (these can be simultaneous)
2. A ramp-up time of 1 to 40ms for VAN and VDD is recommended for best performance
3. VDD should stabilize at least 1ms ahead of VAN
4. The ramp-up time for VPG is not critical and it can be turned on anytime
5. Configure the display registers to the desired startup state
6. Turn on the display by setting the DISPOFF bit in register DISPMODE to “0”

Figure 18 shows the timing diagram for the power supplies and control signals during startup when the display is first turned on. The external supply voltages (VAN, VDD, and VPG) can all be applied at the same time as in the diagram. An internal reset signal (rstn) is triggered when VDD exceeds a built-in threshold level. After a delay of about 40ms the VAN supply to the array is enabled (VANen). Following an additional 20ms the internal dc-dc controller is activated (VCOMen) which generates a negative supply for the common cathode of the array. The video display is enabled 20ms later (VIDEOen) and video is displayed on the array after the DISPOFF bit has been set to “0” via the serial port. Prior to this moment the pixels in the array are actively driven to the black state. The pin RESETB must also be logic high before any registers can be written.

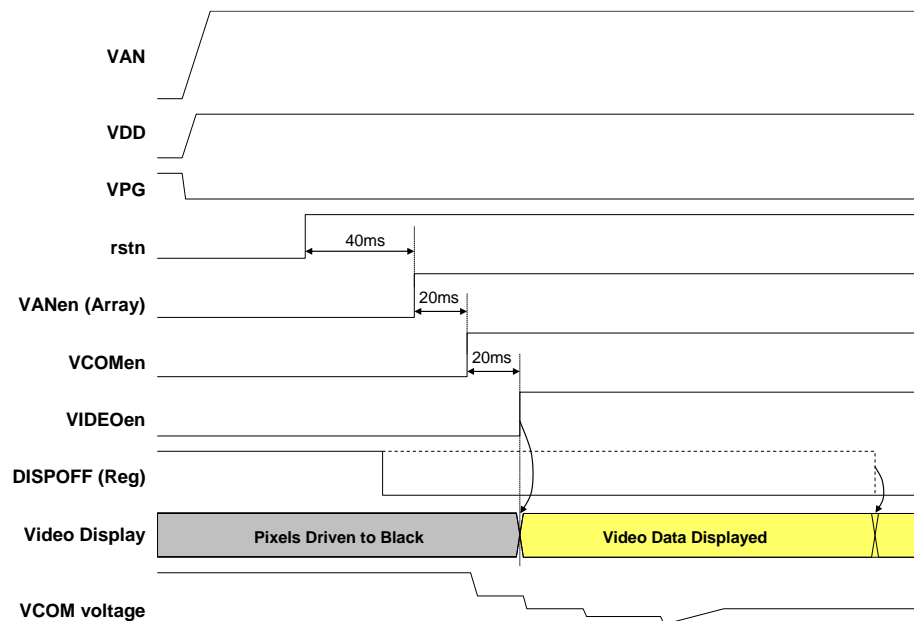


Figure 18 : Power-Up sequence for supplies and control.

NOTE: Do not apply VAN without a VDD supply first. This will result in high current and possible device damage!

The supply currents drawn during a typical startup condition are illustrated in **Error! Reference source not found.**

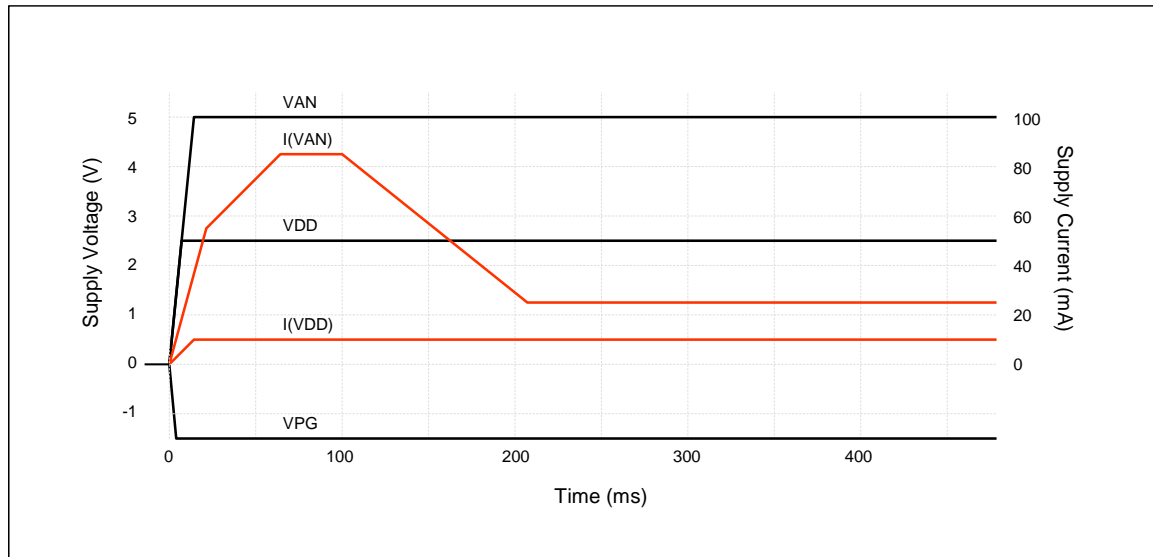


Figure 19: Typical startup currents

9.8 Power-Savings Mode

The display provides power down modes to minimize power consumption. This can occur in two ways:

- Sleep mode – manually controlled via the PDWN bit in register SYSPWRDN, the entire display chip is powered down except for the serial interface. The register settings are saved and restored on power up from this mode.
- Individual block control – several functional blocks have the option to be turned off manually via control of registers ANGPWRDN and SYSPWRDN.

The normal power-down sequence for supplies and control is given in **Error! Reference source not found.**²¹, while the power-down/power-on sequence for the sleep mode is shown in **Error! Reference source not found.** The data, sync and clock inputs should be inactive and held low to achieve the minimum sleep-mode power consumption.

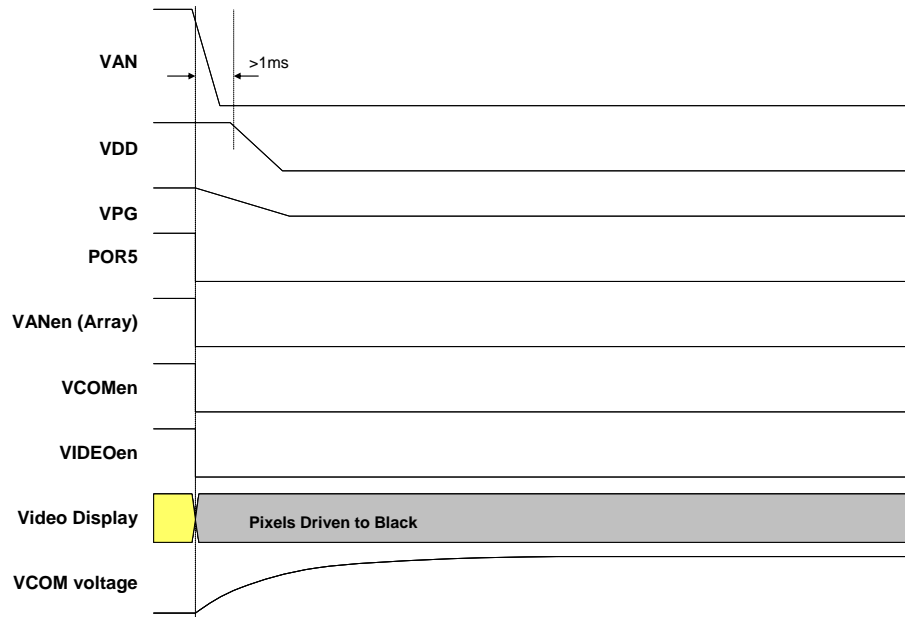


Figure 20: Power-Down sequence for supplies and control.

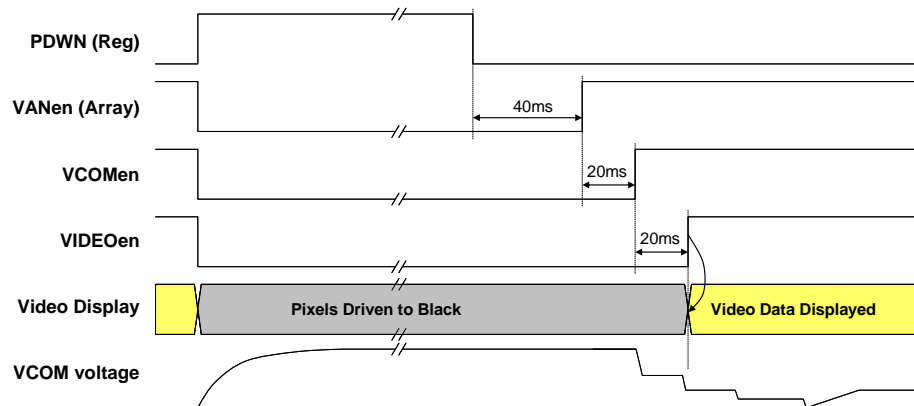


Figure 21: Soft power-down / power-on sequence for supplies and control.

9.8.1 Display-Off Function

On power-up the microdisplay sets all internal registers to their default values and holds the array in the off state (black) until a software reset is externally applied. The DISPOFF bit in the DISPMODE register must be set to zero via the serial port in order for the array to become active.

10. REGISTER MAP SUMMARY

| Address (Hex) | Name | Access | Bit Name | Bit # | Reset Value (Hex) | Description |
|---------------|----------|--------|-------------|-------|-------------------|---|
| 00 | STAT | R | CID | 3 | - | Chip ID (0 = Mono Display Chip, 1 = Color Display Chip) |
| | | | REV | 2-0 | 0 | Silicon Revision Number |
| 01 | VINMODE | R/W | WRDISABLE | 4 | 0 | I ² C Register Write Disable 0 = Write Enable, 1 = Write Protected (All other Regs becomes Read Only) |
| | | | SET_ENABLE | 3 | 0 | ENABLE Active Level 0 = ENABLE active low, 1 = ENABLE active high |
| | | | SET_FIELD | 2 | 0 | FIELD Polarity 0 = Odd Field when ENABLE=Active, 1 = Even Field when ENABLE=Active |
| | | | VSYNCPOL | 1 | 0 | VSYNC Polarity 0 = Negative Sync, 1 = Positive Sync |
| | | | HSYNCPOL | 0 | 0 | HSYNC Polarity 0 = Negative Sync, 1 = Positive Sync |
| 02 | DISPMODE | R/W | DISPOFF | 5 | 1 | Display Off (BURNIN mode override to ON) 0 = Display On, 1 = Display Off |
| | | | 3D-MODE | 4 | 0 | 3D Display Mode 0 = Normal Display, 1 = Time Sequential Mode |
| | | | SCMODE | 3-2 | 0 | Progressive or Interlaced scan mode select 00 = Progressive, 01 = Interlaced, 1X = Pseudo Interlaced |
| | | | VSCAN | 1 | 0 | Vertical Scan Direction 0 = Top to Bottom Scan, 1 = Bottom to Top Scan |
| | | | HSCAN | 0 | 0 | Horizontal Scan Direction 0 = Left to Right Scan, 1 = Right to Left Scan |
| 03 | TOPPOS | R/W | | 5-0 | 14 | Row Display Top Position |
| 04 | BOTPOS | R/W | | 5-0 | 14 | Row Display Bottom Position |
| 05 | ROWRESET | R/W | | 7-0 | 0 | Row Duty Control (0:Disable, Each line displayed ROWRESET*2 Line period) |
| 06 | RAMPCTL | R/W | GCPSAVE | 4 | 0 | Global Counter Power Save Enable 0 = Normal (no power save), 1 = Global Counter power save enable |
| | | | RAMPHIGH | 3 | 0 | Internal Ramp DAC set All High 0 = Normal operation, 1 = DAC set All High |
| | | | FLYBTIME | 2 | 0 | Ramp Fly back Time 0 = 800 nSec, 1 = 500 nSec |
| | | | RAMPDLY | 1-0 | 1 | Ramp Delay by DCLK 00 = -1/2 DCLK, 01 = No Delay, 10 = +1/2 DCLK |
| 07 | RAMPCM | R/W | RAMPMON | 4 | 0 | Internal Ramp Amp Monitor Enable |
| | | | DACMON | 3 | 0 | Internal Ramp DAC Monitor Enable |
| | | | RAMPCM | 2-0 | 4 | Ramp Amp Current Control (000 = -100%(Power down), 001 = -75%, 010 = -50%, 011 = -25%, 100 = ±0%, 101 = +25%, 110 = +50%, 111 = +75%) |
| 08 | VDACMX | R/W | | 7-0 | 0 | Ramp DAC Max Value Control, -40% ~ +40 % |
| 09 | BIASN | R/W | EXT_VREF | 2 | 0 | External VREF Enable |
| | | | BIASN | 1-0 | 1 | 00 = bias current off 01 = bias current set to 0.5nA 10 = bias current set to 1nA |
| 0A | GAMMASET | R/W | PMPHOLD_EN | 4 | 0 | VCOM PUMP hold enable when VGN sampling time 0 = Normal pumping, 1 = Pump hold function enable |
| | | | VGNSH_EN | 3 | 0 | VGN Sample & Hold Enable 0 = VGN SH Bypass, 1 = Enable VGN SH output |
| | | | IDSTEP | 2-0 | 0 | Current level for gamma sensor |
| 0B | VCOMMODE | R/W | ISEN_EN | 3-2 | 0 | VCOM I-Sensor Enable |
| | | | VCOMAUTO | 1-0 | 0 | 00 = AUTO1 mode 01 = AUTO2 mode 10 = MANUAL mode |
| 0C | VCOMCTL | R/W | SS_BYPASS | 7 | 0 | VCOM Soft Start Bypass mode 0 = Soft Start function enable, 1 = Soft Start Bypass |
| | | | VCKDUTY | 6-4 | 3 | VCOM Clock Duty Control (High:Low) 0=1:7, 1=1:3, 2=3:5, 3=1:1, 4=5:3, 5=3:1, 6=7:1, 7=Don't use |
| | | | VCKSEL | 3-2 | 3 | VCOM Clock Select 0=125KHz, 1=250KHz, 2=500KHz, 3=800KHz |
| | | | VCOMSS | 1-0 | 1 | VCOM Soft Start Delay Time Mode 0 = 2mS, 1 = 4mS, 2 = 8mS, 3 = 16mS |
| 0D | VGMAX | R/W | | 7-0 | 0D | Fine adjustment for VGMAX level (default = 4.95V) |
| 0E | VCOM | R/W | | 7-0 | 51 | VCOM manual setting (used when VCOMMODE = 01 or 10 , default = -2.3V) |
| 0F | IDRF | R/W | IDRF_COARSE | 7-5 | 1 | Coarse adjustment for array reference current |
| | | | IDRF_FINE | 4-0 | 10 | Fine adjustment for array reference current |
| 10 | DIMCTL | R/W | | 6-0 | 64 | Dimming level control (default = 1X IDRF) |

| | | | | | | |
|----|----------|-----|----------|-----|----|--|
| 11 | TREFDIV | R/W | | 5-0 | 1E | Temp. Sensor Reference Clock Divider |
| 12 | TEMPOFF | R/W | | 7-0 | 88 | Temp. Sensor Offset |
| 13 | TUPDATE | R/W | | 7-0 | FF | Number of frames per TEMPOUT update (Data range 02H ~ FFH) Update Time = (TUPDATE+1) * PERIOD _{FRAME} PERIOD _{FRAME} = 16.6 mSec when using 60Hz Video |
| 14 | TEMPOUT | RO | | 7-0 | - | Temperature Sensor Readout |
| 15 | ANGPWRDN | R/W | ISENPD | 7 | 0 | ISEN Power Down |
| | | | IDMAXPD | 6 | 0 | IDMAX Power Down |
| | | | VCOMP | 5 | 0 | VCOM Power Down |
| | | | VREFPD | 4 | 0 | VREF Power Down |
| | | | GMPENPD | 3 | 0 | Gamma Sensor Power Down |
| | | | VCMENPD | 2 | 0 | VCOM Sensor Power Down |
| | | | TSENPD | 1 | 0 | Temperature Sensor Power Down |
| | | | TREFPD | 0 | 0 | Temperature Reference Power Down |
| 16 | SYSPWRDN | R/W | PDWN | 4 | 0 | All System Power Down (Override all analog power down, except POR50VPD, POR25VPD) |
| | | | RAMPDP | 3 | 0 | RAMP DAC AMP Power Down |
| | | | DACPD | 2 | 0 | RAMP DAC Power Down |
| | | | POR50VPD | 1 | 0 | 5V POR Power Down |
| | | | POR25VPD | 0 | 0 | 2.5V POR Power Down |
| 17 | TPMODE | R/W | | 2-0 | 0 | Select test pattern for Built-In-Test-Mode (BURNIN pin = 'High') 000= Burn-in (all white), 001=Color Bar, 010=16 level gray scale 011=Checker Board, 100=Vertical Line, 101= Horizontal Line, 110=Grid Pattern |
| 18 | TPLINWTH | R/W | | 7-0 | 0 | Line Test Pattern Line Width (0=1pixel, 1=2pixel, ..., 255=256pixel) |
| 19 | TPCOLSP | R/W | | 7-0 | 0 | Line Test Pattern Column Space (0=1pixel, 1=2pixel, ..., 255=256pixel) |
| 1A | TPROWSP | R/W | | 7-0 | 0 | Line Test Pattern Row Spce (0=1pixel, 1=2pixel, ..., 255=256pixel) |
| 1B | TPCOLOR | R/W | TPBGCLR | 6-4 | 0 | Line Test Pattern Background Color (RGB) |
| | | | TPFGCLR | 2-0 | 7 | Line Test Pattern Forground Color (RGB) |
| 1C | DIGTEST | R/W | | 7 | 0 | FB_FAST |
| | | | | 6 | 0 | FB_SLOW |
| | | | | 5 | 0 | SETB_EN |
| | | | | 4 | 0 | CPREQ_IN |
| | | | | 3 | 0 | TEST_EN |
| | | | | 2 | 0 | CTST RESET |
| | | | | 1-0 | 0 | TESTMODE |
| 2E | PUCTRL | R/W | PUCEN | 3 | 0 | Auto Power-Up sequence override Enable |
| | | | VIDEN | 2 | 0 | Video Display Enable |
| | | | VCMEN | 1 | 0 | VCOM Enable |
| | | | VANEN | 0 | 0 | VAN Enable |
| 2F | HIDDEN | R/W | | 2 | 0 | VCOM OSC enable |
| | | | | 1 | 0 | STB_EN_IN polarity invert |
| | | | | 0 | 0 | ROW_ODDSEL_IN polarity invert |

11. DETAILED REGISTER DESCRIPTIONS

11.1 STAT (00h)

| | |
|----------------|-----------|
| Name | STAT |
| Address | 00h |
| Mode | Read Only |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|---------------------------------------|
| CID | 3 | - | Indicates monochrome or color display |
| REV | 2-0 | 0 | Silicon revision number; Rev. 1 = 0 |

Bits REV in this register indicate the revision number of the silicon backplane design, with 0 corresponding to the first silicon known as Rev. 1.

Bit CID indicates the version of silicon backplane with “0” for a monochrome display and “1” for the color version.

11.2 VINMODE (01h)

| | |
|----------------|--------------|
| Name | VINMODE |
| Address | 01h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|------------|------|-------------|---|
| WRDISABLE | 4 | 0 | I ² C register write disable |
| SET_ENABLE | 3 | 0 | ENABLE active level |
| SET_FIELD | 2 | 0 | Field polarity |
| VSYNCPOL | 1 | 0 | VSYNC polarity |
| HSYNCPOL | 0 | 0 | HSYNC polarity |

WRDISABLE:

- 1 = write protected (all other registers become read only)
- 0 = write enable (all registers can be updated externally via I²C) (default)

SET_ENABLE:

- 0 = the active state of the ENABLE input is set “low” (default)
- 1 = the active state of the ENABLE input is set “high”

The ENABLE input pin is used to implement 3D video modes using a single RGB source, with two consecutive frames carrying information for each eye. The microdisplay can be programmed for either an active high or low ENABLE input using the SET_ENABLE bit, allowing a single video signal to be used with two displays. In such a configuration, one display scans and displays, while the other one holds and displays. The active state of the ENABLE input corresponds to the video data being scanned and displayed by the microdisplay.

To implement the Frame Sequential 3D Mode according to the VESA Standard for Stereoscopic Display Hardware, the display for the left eye is programmed with SET_ENABLE=1 and the right eye display is programmed with SET_ENABLE=0. Consequently, the data for the left eye is supplied and displayed when ENABLE=1 while the display for the right eye displays the previous frame of data.

The ENABLE input pin is also used to indicate field polarity in non-3D interlaced modes. In this mode the SET_FIELD bit determines the field polarity when ENABLE is active.

SET_FIELD:

- 0 = Odd Field when ENABLE=Active (default)
- 1 = Even Field when ENABLE=Active

The SET_FIELD register determines the field polarity of the video signal when the ENABLE pin is active.

VSYNCPOL:

- 0 = Negative Sync (default)
- 1 = Positive Sync

HSYNCPOL:

- 0 = Negative Sync (default)
- 1 = Positive Sync

The SYNCPOL registers are used to determine whether the positive or negative edge of the external synchronization clocks (HSYNC and VSYNC) is used as the active transition by the internal display sequencers and control logic.

11.3 DISPMODE (02h)

| | |
|----------------|--------------|
| Name | DISPMODE |
| Address | 02h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|---|
| DISPOFF | 5 | 1 | Display On/Off control |
| 3D-MODE | 4 | 0 | 3D Mode control |
| SCMODE | 3-2 | 0 | Progressive or Interlaced scan mode selection |
| VSCAN | 1 | 0 | Vertical Scan direction |
| HSCAN | 0 | 0 | Horizontal Scan direction |

DISPOFF:

- 0 = Display is turned ON
- 1 = Display is turned OFF (default)

The display starts in the OFF state by default and requires a command via the serial port to be turned on.

3D-MODE:

- 0 = Normal display mode (default)
- 1 = Time Sequential 3D mode

These bits are used to set the 3D mode of operation in conjunction with SET_ENABLE (bit #3 of the VINMODE register) and the Enable input. In Frame Sequential Mode each video frame contains information for either the left or right eye. When 3D-MODE="1" the SCMODE bit in the DISPMODE register is overridden to Progressive Scan Mode (0h). The following description for Frame Sequential operation assumes the source is in compliance with the VESA standard, where the data for the left eye is provided while the Enable signal is at the logic high level, and the data for the right eye display is provided while the Enable signal is at the logic low level. The Enable input signal is sampled into the circuit by a flip-flop clocked on the falling edge of VSYNC and the sampled value is used for the next frame. (The Enable signal is generated by the graphics software and may not be synchronized to the VSYNC signal).

To activate the stereovision mode, the right eye display needs to be configured with Enable active low (SET_ENABLE= "0", bit #3 of the VINMODE register). This will allow the right eye microdisplay to hold the previous frame while the Enable input is high. The left eye display needs to be configured with Enable active high (SET_ENABLE="1", bit #3 of the VINMODE register). Thus the two Enable inputs can be tied together to the incoming Stereo Sync signal provided by the graphics adapter (or other custom source).

SCMODE:

- 00 = Progressive scan mode (default)
- 01 = Interlaced scan mode
- 1X = Pseudo-interlaced mode

Interlaced modes are limited to a maximum of 512 and a minimum of 240 active rows per field.

VSCAN:

- 0 = Top to Bottom vertical scan direction (default)
- 1 = Bottom to Top vertical scan direction

HSCAN:

- 0 = Left to Right horizontal scan direction (default)
- 1 = Right to Left horizontal scan direction

11.4 TOPPOS (03h)

| | |
|----------------|--------------|
| Name | TOPPOS |
| Address | 03h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|----------------------------------|
| | 5-0 | 14 | Top position of first active row |

This register, along with register BOTPOS, is used to set the vertical position of the active display window within the 520 available rows of pixels. In VGA mode the active window can be moved by +/-20 pixels from the center (default) position. When TOPPOS is increased, register BOTPOS must be decreased by the same value so that the sum of the two remains equal.

11.5 BOTPOS (04h)

| | |
|----------------|--------------|
| Name | BOTPOS |
| Address | 04h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|------------------------------------|
| | 5-0 | 14 | Bottom position of last active row |

This register, along with register TOPPOS, is used to set the vertical position of the active display window within the 520 available rows of pixels. In VGA mode the active window can be moved by +/-20 pixels from the center (default) position. When TOPPOS is increased, register BOTPOS must be decreased by the same value so that the sum of the two remains equal.

11.6 ROWRESET (05h)

| | |
|----------------|--------------|
| Name | ROWRESET |
| Address | 05h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|-----------------------|
| | 7-0 | 0 | Row duty rate control |

This register is used to set the number of line cycles (in steps of 2) during which each row is active in any frame period. Each row is driven to black during the non-active line cycles.

| ROWRESET (dec) | Active Line Cycles | Active Duty Rate (%) | Note |
|----------------|--------------------|---------------------------------|---------------------------------------|
| 0 | all | 100 | Pixels active for entire frame period |
| 1 | 2 | $2 \cdot T_{HSYNC} / T_{FRAME}$ | Total HS cycles / frame |

| | | | |
|------|-----|---------------------------|---------------------------------------|
| n | 2*n | $2*n*T_{HSYNC}/T_{FRAME}$ | |
| >254 | all | 100 | Pixels active for entire frame period |

11.7 RAMPCTL (06h)

| | |
|----------------|--------------|
| Name | RAMPCTL |
| Address | 06h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|----------------------------------|
| GCPSAVE | 4 | 0 | Global counter power save enable |
| RAMPHIGH | 3 | 0 | Set internal RAMP DAC high |
| FLYBTIME | 2 | 0 | RAMP Flyback time |
| RAMPDLY | 1-0 | 1 | RAMP delay in DCLK cycles |

GCPSAVE:

- 0 = Power save mode disable (default)
- 1 = Power save mode enable

The GCPS register is used to enable the Global Counter power saving option in which the internal D/A converter operates in a hybrid 8-bit/10-bit conversion mode.

RAMPHIGH:

- 0 = Normal operation (default)
- 1 = DAC set to all high output

The RAMPHIGH register is used to set internal RAMPDAC to all high output mode for test purposes.

FLYBTIME:

- 0 = 500 ns (default)
- 1 = 800 ns

The FLYBTIME register is used to set the fly-back time for the internal RAMP.

RAMPDLY:

- 00 = - 1/2 DLCK
- 01 = no delay (default)
- 10 = + 1/2 DCLK

The RAMPDLY2 register is used to adjust the starting position of the internal RAMP.

11.8 RAMPCM (07h)

| | |
|-------------|--------|
| Name | RAMPCM |
|-------------|--------|

| | |
|----------------|--------------|
| Address | 07h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|----------------------------------|
| RAMPMON | 4 | 0 | Internal RAMP Amp monitor enable |
| DACMON | 3 | 0 | Internal RAMP DAC monitor enable |
| RAMPCM | 2-0 | 4 | RAMP Amp current control |

RAMPMON:

- 0 = Disable internal RAMP Amp monitoring (default)
- 1 = Enable internal RAMP Amp monitoring

The RAMPMON register is used to enable monitoring of the internal RAMP amplifier output signal.

DACMON:

- 0 = Disable internal RAMP DAC monitoring (default)
- 1 = Enable internal RAMP DAC monitoring

The DACMON register is used to enable testing of the internal RAMP DAC output signal.

RAMPCM:

- 000 = -100% (power down)
- 001 = -75%
- 010 = -50%
- 011 = -25%
- 100 = nominal (default)
- 101 = +25%
- 110 = +50%
- 111 = +75%

The RAMPCM register is used to set the operating bias current for the internal RAMP amplifier. The settings reduce or increase the current by a percentage of the nominal (default) value.

11.9 VDACMX (08h)

| | |
|----------------|--------------|
| Name | VDACMX |
| Address | 08h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|--------------------------------|
| | 7-0 | 0 | RAMP DAC maximum value control |

Register VDACMX is used to adjust the maximum value of the internal RAMP DAC signal by -40% to +40% of the nominal value.

NOTE: The normal operating value for VDACMX should be set to 78h.

The typical dependence of display luminance on VDACMX(dec) is shown in Figure 22. The luminance is seen to saturate for VDACMX greater than 79h in this sample. For normal operation VDACMX should be set to about 90 to 95% of the saturation value as shown in the figure.

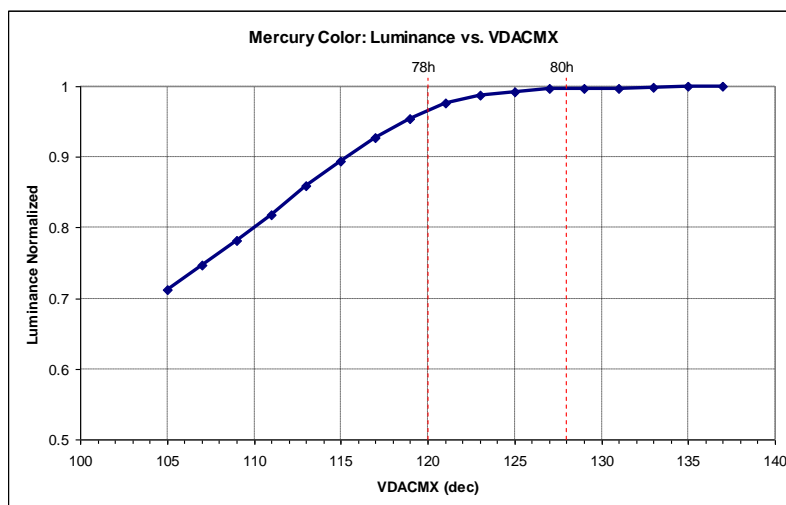


Figure 22: Luminance dependency on VDACMX

11.10 BIASN (09h)

| | |
|----------------|--------------|
| Name | BIASN |
| Address | 09h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|------------------------|
| EXT_VREF | 2 | 0 | Enable external VREF |
| BIASN | 1-0 | 1 | Set pixel bias current |

EXT_VREF:

- 1 = enable the external VREF source
- 0 = use the internal VREF source (default)

Note: This option not available on the current package – use the default setting only.

BIASN:

- 00 = pixel bias current is turned off
- 01 = pixel bias current set to 0.5nA (default)
- 10 = pixel bias current set to 1nA

The BIASN register is used to set the sink current applied in each pixel cell. It is recommended to use the BIASN=01 setting in normal operation.

11.11 GAMMASET (0Ah)

| | |
|----------------|--------------|
| Name | GAMMASET |
| Address | 0Ah |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|------------|------|-------------|--------------------------------|
| PMPHOLD_EN | 4 | 0 | VCOM pump hold enable |
| VGNSH_EN | 3 | 0 | VGN sample & hold enable |
| IDSTEP | 2-0 | 0 | Current level for gamma sensor |

PMPHOLD_EN:

- 0 = Normal operation, pump hold disabled (default)
- 1 = Enable pump hold during VGN sampling time

The PMPHOLD_EN register is used to disable the VCOM converter switch during the VGN sampling time to reduce noise pickup.

VGNSH_EN:

- 0 = Bypass the VGN sample & hold function (default)
- 1 = Enable the VGN sample & hold function

The VGNSH_EN register is used to activate the internal sample & hold function provided at the VGN output pin.

IDSTEP:

- 0h \approx IDRF/128
- 1h \approx IDRF/64
- 2h \approx IDRF/32
- 3h \approx IDRF/16
- 4h \approx IDRF/8
- 5h \approx IDRF/4
- 6h \approx IDRF/2
- 7h = IDRF

The IDSTEP register is used to set the current level for the gamma sensor. The corresponding output voltage is provided at pin VGN.

A minimum of 10msec following an IDSTEP register update should be allowed for the VGN signal to settle before sampling. In addition, sampling of the VGN signal should be carried out during the Frame Blanking time.

11.12 VCOMMODE (0Bh)

| | |
|----------------|--------------|
| Name | VCOMMODE |
| Address | 0Bh |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|--------------------------------|
| ISEN_EN | 3-2 | 0 | Enable the VCOM current sensor |
| VCOMAUTO | 1-0 | 0 | Set internal VCOM supply mode |

ISEN_EN:

TBD

VCOMAUTO:

This register sets the operating mode of the internal VCOM dc-dc converter.

- 00 = AUTO1 mode (default)
- 01 = AUTO2 mode
- 10 = MANUAL mode

In the AUTO1 mode, the VCOM converter uses an internal current reference to maintain a fixed OLED current level, which is defined by registers DIMCTL and IDRFB.

In the AUTO2 mode, the VCOM converter regulates the OLED current level when the VCOM supply is below a set threshold (defined by the VCOM register), and clamps the output to the threshold level when conditions call for a VCOM output above the threshold level.

In the Auto 3 mode, the VCOM converter uses a voltage reference signal to maintain a fixed cathode supply voltage. The value of the cathode voltage is set by register VCOM.

11.13 VCOMCTL (0Ch)

| | |
|----------------|--------------|
| Name | VCOMCTL |
| Address | 0Ch |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|-----------|------|-------------|---------------------------------|
| SS_BYPASS | 7 | 0 | Bypass the VCOM soft start mode |
| VCKDUTY | 6-4 | 3 | VCOM clock duty control |
| VCKSEL | 3-2 | 3 | VCOM clock select |
| VCOMSS | 1-0 | 1 | VCOM soft start delay time |

SS_BYPASS:

- 0 = Normal operation, soft-start function enabled (default)
- 1 = Disable the VCOM soft-start function

VCKDUTY:

- 0h = 1:7
- 1h = 1:3
- 2h = 3:5
- 3h = 1:1 (default)
- 4h = 5:3
- 5h = 3:1
- 6h = 7:1
- 7h = don't use

Register VCKDUTY sets the VCOM clock duty ratio (high:low).

VCKSEL:

- 0h = 125 kHz
- 1h = 250 kHz
- 2h = 500 kHz
- 3h = 800 kHz (default)

Register VCKSEL sets the operating frequency of the VCOM clock.

VCOMSS:

- 0h = 2 ms
- 1h = 4 ms (default)
- 2h = 8 ms
- 3h = 16 ms

Register VCMOSS sets the soft-start duration during startup of the VCOM converter.

11.14 VGMAX (0Dh)

| | |
|----------------|--------------|
| Name | VGMAX |
| Address | 0Dh |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|---------------------------------|
| | 7-0 | 0D | Fine adjustment for VGMAX level |

- 00h = 5 (VAN = 5V)
- 0Dh = 4.95 (default)

$$\text{FFh} = 4$$

$$\text{VGMAX level} = \text{VAN} * (1 - 0.2 * \text{VGMAX(dec)} / 255)$$

This register sets the pixel voltage at which the maximum OLED current is regulated. It should be slightly below the VAN supply to prevent saturation of the video buffer amplifiers.

11.15 VCOM (0Eh)

| | |
|----------------|--------------|
| Name | VCOM |
| Address | 0Eh |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|---------------------|
| | 7-0 | 51 | VCOM manual setting |

Cathode supply as a function of VCOM setting:

| VCOM(h) | FF | F0 | E0 | D0 | C0 | B0 | A0 | 90 | 80 | 70 | 60 | 51* | 40 | 30 |
|---------|------|------|------|------|------|------|-----|-----|------|-----|-----|-----|------|------|
| Voltage | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | 0.29 | 0.38 | 0.47 | 0.59 | 0.72 | 0.85 | 1.0 | 1.2 | 1.43 | 1.7 | 2.0 | 2.4 | 2.97 | 3.68 |

*default value

Register VCOM[7,0] sets the fixed output level for the internal VCOM inverter when VCOMMODE =01 or 10. There is no compensation for the variation in OLED behavior with temperature in this mode of operation. As a result, a setting at room temperature will not necessarily result in optimal contrast and the same luminance at other temperatures. The default setting (51h) will result in a cathode supply \approx -2.3V. The typical dependency of luminance on the VCOM setting in manual mode is given in Figure 23 for a color display.

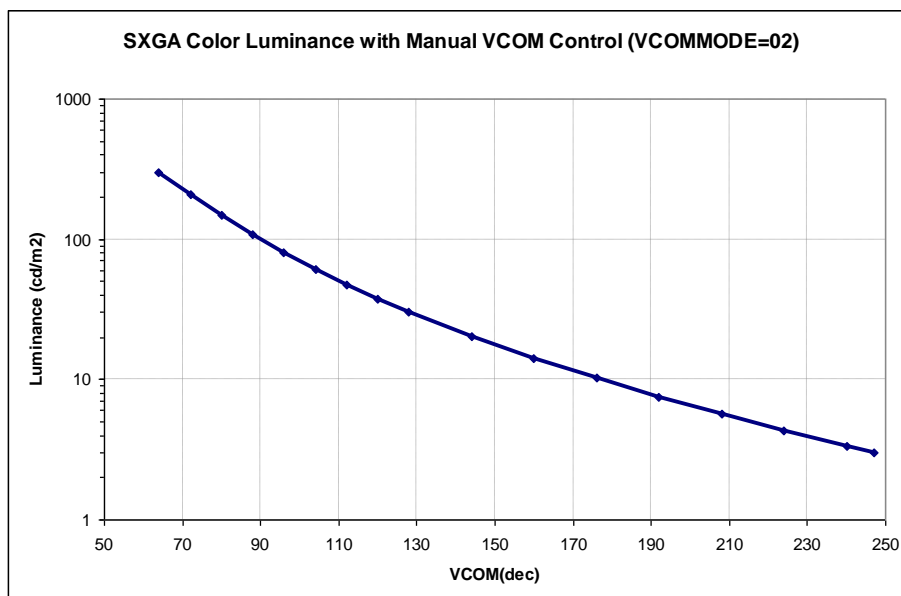


Figure 23: Typical luminance dependency on manual VCOM setting

11.16 IDRF (0Fh)

| | |
|---------|--------------|
| Name | IDRF |
| Address | 0Fh |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|-------------|------|-------------|---|
| IDRF_COARSE | 7-5 | 1 | Coarse adjustment for array reference current |
| IDRF_FINE | 4-0 | 10 | Fine adjustment for array reference current |

IDRF_COARSE:

IC#
0h = 0
1h = 0.5 (default)
2h = 1.5
3h = 2.5
4h = 3.5

IDRF_FINE:

IF#
00h = 0
01h = 1/32
...
10h = 16/32 (default)
...
1Fh = 31/32

Register IDRF is used to set the maximum OLED current, which determines the luminance level for the display. The luminance will be directly proportional to the IDRF factor (sum of IC# and IF#) and the reference luminance LDEF given by the following expression:

$$LMAX = LDEF * (IC\# + IF\#) \quad \text{in cd/m}^2$$

where the luminance for a monochrome green display is $LDEF \approx 1500 \text{ cd/m}^2$ at the default settings (see table below).

| IDRF (hex) | LMAX / LDEF |
|------------|-------------|
| 0 | 0 |
| 10 | 0.5 |
| 20 | 0.5 |
| 30 | 1 (default) |
| 40 | 1.5 |
| 50 | 2 |
| 60 | 2.5 |
| 70 | 3 |
| 80 | 3.5 |

11.17 DIMCTL (10h)

| | |
|----------------|--------------|
| Name | DIMCTL |
| Address | 10h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|-----------------------|
| | 6-0 | 64 | Dimming level control |

00h = 0

01h = 1% of LMAX

...

64h = 100% of LMAX

...

7Fh = 127% of LMAX

This register provides linear control of the display luminance level ranging from 0 to 127% in steps of 1%. The default value of 64h is equal to 100% of the luminance defined by register IDRF.

This register is only operational in Auto VCOM mode (VCOMMODE=00).

11.18 TREFDIV (11h)

| | |
|----------------|--------------|
| Name | TREFDIV |
| Address | 11h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|---|
| | 5-0 | 1E | Temperature sensor reference clock divider adjust |

The register TREFDIV is used to adjust the slope of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -40 to 80°C, although the setting is best determined by a calibration measurement of the display in its final assembly.

See the description for register TEMPOUT.

11.19 TEMPOFF (12h)

| | |
|----------------|--------------|
| Name | TEMPOFF |
| Address | 12h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|----------------------------------|
| | 7-0 | 88 | Temperature sensor offset adjust |

The register TEMPOFF is used to adjust the offset of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -40 to 80°C, although the setting is best determined by a calibration measurement of the display in its final assembly.

See the description for register TEMPOUT.

11.20 TUPDATE (13h)

| | |
|----------------|--------------|
| Name | TUPDATE |
| Address | 13h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|-------------------------------------|
| | 7-0 | FF | Number of frames per TEMPOUT update |

This register sets the update rate of the Temperature Sensor reading, TEMPOUT. The time between sensor updates is given by:

$$\text{Update Time} = (\text{TUPDATE}(\text{decimal}) + 1) * T_{\text{FRAME}}$$

where the frame period T_{FRAME} is equal to 16.6 ms for 60Hz video. The valid range for TUPDATE is 02h to FFh.

11.21 TEMPOUT (14h)

| | |
|----------------|-----------|
| Name | TEMPOUT |
| Address | 14h |
| Mode | Read Only |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|----------------------------|
| | 7-0 | - | Temperature sensor readout |

Register TEMPOUT provides an 8bit digital output that is linearly proportional to the chip temperature. The VGA display temperature sensor is designed around a P-N junction. The output of the junction is sampled by an internal current to voltage converter, digitized and stored into a dedicated 8-bit register TEMPOUT. The sampling rate is controlled by configuration register TUPDATE (13H). By default the temperature sensor is updated once every 255 frames. Two registers are used to set the sensor gain (TREFDIV) and sensor offset (TEMPOFF). The temperature sensor can be powered down when not used by setting TSENPD =1 in the PWRDN register.

The temperature sensor is intended to provide a full-scale reading over a temperature range defined by the user. Assuming that the desired operating temperature range is defined by T_{MIN} and T_{MAX} , the expected sensor response would be as follows:

$$TEMPOUT(dec) = A * temp + B$$

where temp is the chip temperature in degrees Celsius, and A and B are given by:

$$A = \frac{255}{T_{MAX} - T_{MIN}}$$

$$B = \frac{-255 * T_{MIN}}{T_{MAX} - T_{MIN}}$$

The actual sensor response is determined by registers TREFDIV and TEMPOFF through the following relationship:

$$TEMPOUT(d) = k_1 * TREFDIV(d) * temp + k_2 + TEMPOFF(d)$$

The constants k_1 and k_2 are dependent on properties of the silicon and package assembly. For example, the average register settings needed to achieve a working temperature range of -60°C to +80°C are given by the following values:

$$TREFDIV(d) = 25$$

$$TEMPOFF(d) = 93$$

Using these values will result in a variation in temperature reading from part to part due to manufacturing tolerances. To get a reasonably good sensor performance it is usually enough to just find the optimum

value for TEMPOFF which requires only one measurement at room temperature. Increased accuracy can be obtained for a specific part by performing the calibration measurements described below.

To find the optimum value for TREFDIV do the following:

- Place the display in a temperature controlled environment, e.g. an oven
- Set TREFDIV=25d=19h and TEMPOFF=0
- Set DISPMODE=20h (turn off the display)
- Read TEMPOFF at several ambient temperatures, e.g. 0°C, 20°C, 40°C, 60°C
- Take the slope to find the sensor response, $A_{MEAS} = d\text{TEMPOUT}(d)/d\text{temp}$
- The optimum value for TREFDIV is then given by

$$TREFDIV_{OPT} = 25 * \frac{1.82}{A_{MEAS}}$$

To find the optimum value for TEMPOFF do the following:

- Set TREFDIV=25d=19h (or the optimum value) and TEMPOFF=0
- Set DISPMODE=20h (turn off the display)
- Allow several minutes to stabilize and then read TEMPOUT_{AMB} and the ambient temperature T_{AMB}
- The optimum value for TEMPOFF is then given by

$$TEMPOFF_{OPT} = 1.82 * T_{AMB} + 109 - TEMPOUT_{AMB}$$

With these settings, the microdisplay temperature can be found from the sensor reading through the following relationship:

$$T(^{\circ}\text{C}) = \frac{140}{255} * TEMPOUT(d) - 60$$

Temperatures below -60°C will return a TEMPOUT reading of 0 and temperatures above +80°C will return a hexadecimal value of FF.

11.22 ANGPWRDN (15h)

| | |
|----------------|--------------|
| Name | ANGPWRDN |
| Address | 15h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|-----------------|
| ISENPD | 7 | 0 | ISEN power down |

| | | | |
|---------|---|---|----------------------------------|
| IDMAXPD | 6 | 0 | IDMAX power down |
| VCOMPDP | 5 | 0 | VCOM power down |
| VREFPD | 4 | 0 | VREF power down |
| GMSENPD | 3 | 0 | Gamma sensor power down |
| VCSENPD | 2 | 0 | VCOM sensor power down |
| TSENDP | 1 | 0 | Temperature sensor power down |
| TREFPD | 0 | 0 | Temperature reference power down |

ISENPD:

1 = VCOM current limit sensor is powered down
0 = normal operation (default)

IDMAXPD:

1 = IDMAX function is powered down
0 = normal operation (default)

VCOMPDP:

1 = VCOM generator is powered down
0 = normal operation (default)

VREFPD:

1 = the VREF reference source is powered down
0 = normal operation (default)

GMSENPD:

1 = the Gamma sensor is powered down
0 = normal operation (default)

VCSNEPD:

1 = the VCOM sensor is powered down
0 = normal operation (default)

TSENDP:

1 = the Temperature Sensor is powered down
0 = the Temperature Sensor is operating normally (default)

TREFPD:

1 = the Temperature reference is powered down
0 = normal operation (default)

11.23 SYSPWRDN (16h)

| | |
|------|----------|
| Name | SYSPWRDN |
|------|----------|

| | |
|----------------|--------------|
| Address | 16h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|--------------------------------|
| PDWN | 4 | 0 | All systems power down |
| RAMPPD | 3 | 0 | RAMP DAC amp power down |
| DACPD | 2 | 0 | RAMP DAC power down |
| POR50VPD | 1 | 0 | 5V power-on-reset power down |
| POR25VPD | 0 | 0 | 2.5V power-on-reset power down |

PDWN:

- 1 = all systems are powered down
- 0 = normal operation (default)

By setting the PDWN bit to a “1” the chip enters a deep sleep mode in which all functions including the I²C interface are powered down in order to minimize power consumption. The data, sync and clock inputs should be inactive and held low to achieve the lowest power consumption. An on-chip Address Detection circuit monitors the I²C input lines and resets the PDWN bit when it detects the correct I²C address, restoring the display to operating mode.

All register settings are saved in the power down mode and the display will restart in its previous state when normal operation is resumed.

RAMPPD:

- 1 = internal RAMP DAC amplifier is powered down
- 0 = normal operation (default)

DACPD:

- 1 = internal RAMP DAC is powered down (use when external RAMP option is enabled)
- 0 = internal RAMP DAC is operational (default)

The internal RAMP DAC generator may be power down if an external RAMP source is used.

POR50VPD:

- 1 = the 5V power-on-reset circuit is powered down
- 0 = normal operation (default)

POR25VPD:

- 1 = the 2.5V power-on-reset circuit is powered down
- 0 = normal operation (default)

11.24 TPMODE (17h)

| | |
|----------------|--------------|
| Name | TPMODE |
| Address | 17h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|--------------------------------------|
| | 2-0 | 0 | Select test pattern for Burn-In mode |

The BI pin must be tied high to activate the Burn-In test mode which can be used to check display functionality without the presence of external video data or clock signals. In this mode the display generates data, syncs and the pixel clock internally for several different video patterns. The TPMODE register is used to select one of the built-in test patterns in Burn-In mode via the serial interface.

000 = all white pattern (default)
 001 = color bars
 010 = gray scale (without gamma correction)
 011 = checkerboard pattern
 100 = alternating columns pattern
 101 = alternating rows pattern
 110 = grid pattern
 101 = all black

Use with registers TPLINWTH, TPCOLSP, TPROWSP and TPCOLOR to modify the patterns according to the following table.

| Test Pattern Name | TPMODE (17H) | TPLINWTH (18H) | TPCOLSP (19H) | TPROWSP (1AH) | TPFGCLR (1BH:2-0) | TPBGCLR (1BH:6-4) |
|--------------------|--------------|----------------|---------------|---------------|-------------------|-------------------|
| All White | 000 | X | X | X | X | X |
| Color Bar | 001 | X | X | X | X | X |
| Gray Scale | 010 | X | X | X | X | X |
| Checker Board | 011 | X | X | X | X | X |
| Alternating Column | 100 | LW | CS | X | 111 | 000 |
| Alternating Row | 101 | LW | X | RS | 111 | 000 |
| Grid Pattern | 110 | LW | CS | RS | 111 | 000 |
| All Black | 101 | X | X | X | 000 | 000 |
| All White | 101 | X | X | X | 111 | 111 |
| All Red | 101 | X | X | X | 100 | 100 |
| All Green | 101 | X | X | X | 010 | 010 |
| All Blue | 101 | X | X | X | 001 | 001 |

X: Don't care, LW: Line Width (0~255), CS: Column Space (0~255), RS: Row Space (0~255)

11.25 TPLINWTH (18h)

| | |
|----------------|--------------|
| Name | TPLINWTH |
| Address | 18h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|-------------------------|
| | 7-0 | 0 | Test pattern line width |

This register is used to set the line width for the line-type test patterns.

0 = 1 pixel wide (default)
 1 = 2 pixel wide
 ...
 255 = 256 pixel wide

11.26 TPCOLSP (19h)

| | |
|----------------|--------------|
| Name | TPCOLSP |
| Address | 19h |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|-----------------------------|
| | 7-0 | 0 | Test pattern column spacing |

This register is used to set the column spacing for the column-type test patterns.

0 = 1 pixel space (default)
 1 = 2 pixel space
 ...
 255 = 256 pixel space

11.27 TPROWSP (1Ah)

| | |
|----------------|--------------|
| Name | TPROWSP |
| Address | 1Ah |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|--------------------------|
| | 7-0 | 0 | Test pattern row spacing |

This register is used to set the row spacing for the row-type test patterns.

0 = 1 pixel space (default)

1 = 2 pixel space
...
255 = 256 pixel space

11.28 TPCOLOR (1Bh)

| | |
|----------------|--------------|
| Name | TPCOLOR |
| Address | 1Bh |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|-------------------------------|
| TPBGCLR | 6-4 | 0 | Test pattern background color |
| TPFGCLR | 2-0 | 7 | Test pattern foreground color |

This register is used to set the background and foreground colors (RGB) for certain test patterns.

11.29 DIGTEST (1Ch)

| | |
|----------------|--------------|
| Name | DIGTEST |
| Address | 1Ch |
| Mode | Read / Write |

This register is used test purposes only and should not be modified by the user.

11.30 PUCTRL (2Eh)

| | |
|----------------|--------------|
| Name | PUCTRL |
| Address | 2Eh |
| Mode | Read / Write |

| Bit Name | Bit# | Reset Value | Description |
|----------|------|-------------|--|
| PUCEN | 3 | 0 | Auto Power-up sequence override enable |
| VIDEN | 2 | 0 | Video display enable |
| VCMEN | 1 | 0 | VCOM enable |
| VANEN | 0 | 0 | VAN enable |

These registers can be used to create a customized power-up sequence.

11.31 HIDDEN (2Fh)

| | |
|----------------|--------------|
| Name | HIDDEN |
| Address | 2Fh |
| Mode | Read / Write |

This register is used for test purposes only and should not be modified by the user.

12. APPENDIX A: APPLICATION SYSTEM DIAGRAM

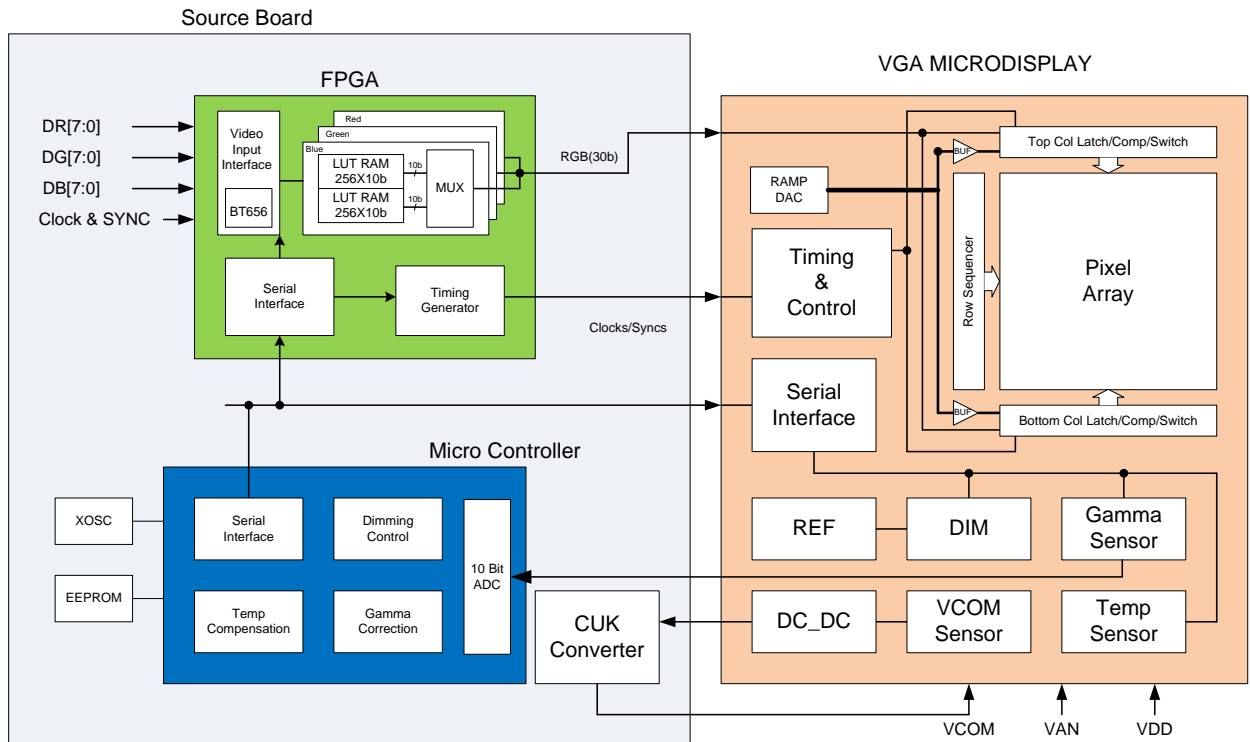


Figure 24: Block diagram of application reference system

13. APPENDIX B: MICRODISPLAY CARRIER BOARD

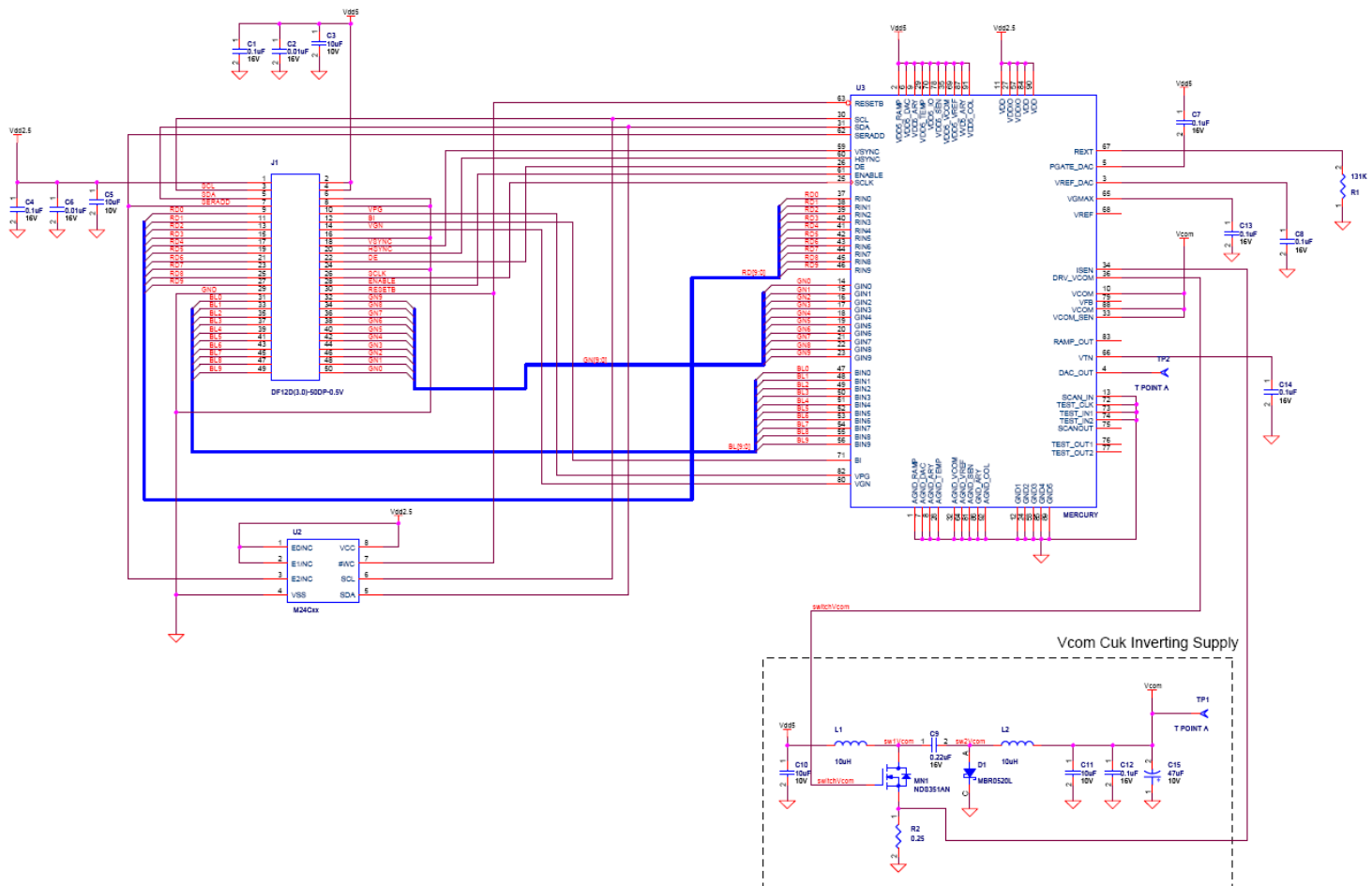


Figure 25: Carrier board schematic (D01-500588-01)

14. APPENDIX C: TYPICAL REGISTER SETTING

The screenshot shows the Mercury Design Reference Kit Software V1.1 interface. The top bar includes a menu (File, CommPort, Bootloader), a version dropdown (0.2), the eMagin logo, a brightness slider (set to 64), a status button, and three mode buttons (OLED, FPGA, VPG). The main area is divided into three sections: OLED, FPGA, and Gamma Coefficients GC().

OLED Section:

| | | | | | |
|----------|----|----------|----|----------|----|
| STATUS | 00 | VCOMCTL | 3D | TPLINWTH | 00 |
| VINMODE | 00 | VGMAX | 0D | TPCOLSP | 00 |
| DISPMODE | 00 | VCOM | 51 | TPROWSP | 00 |
| TOPPOS | 14 | IDRF | 30 | TPCOLOR | 07 |
| BOTPOS | 14 | DIMCTL | 64 | DIGTEST | 00 |
| ROWRESET | 00 | TREFDIV | 1E | PUCTRL | 00 |
| RAMPCTL | 01 | TEMPOFF | 88 | | 47 |
| RAMPCM | 04 | TUPDATE | FF | | |
| VDACMAX | 78 | TEMPOUT | 8E | | |
| BIASN | 01 | ANGPWRDN | 00 | | |
| GAMMASET | 00 | SYSPWRDN | 00 | | |
| VCOMMODE | 00 | TPMODE | 00 | | |

FPGA Section:

| | |
|-----------|----|
| STATE | 01 |
| VIDMODE | 20 |
| ADDR | 04 |
| WRDATA_L | 00 |
| WRDATA_H | 01 |
| LUTRDY | 00 |
| SYNCPOL | 07 |
| RAMPCTL | 00 |
| DACTEST | 00 |
| 3DControl | 00 |

Gamma Coefficients GC() Section:

| | | |
|---|------|---------|
| 8 | 1023 | Read |
| 7 | 930 | Write |
| 6 | 820 | System |
| 5 | 740 | |
| 4 | 640 | |
| 3 | 560 | 1.6 |
| 2 | 500 | Set |
| 1 | 460 | Presets |
| 0 | 01 | |

Buttons: Read, Write, Update LUT, Read LUT.

Messages:

Status: Port 1, 9600,n,8,1 **00:03:00**

Figure 26: Recommended Register Settings for Normal Operation

15. APPENDIX D: EEPROM MEMORY MAP

Each VGA microdisplay contains an EEPROM memory device to serve as non-volatile data storage for retrieving display specific information, such as its serial number and optimal registers values for proper operation. The data can be accessed via the same I²C serial interface that is used to communicate with the microdisplay. The device's serial address is as follows:

Write Mode: Address is A6h (or AEh if SERADD = 1) – *Prohibited mode*

Read Mode: Address is A7h (or AFh if SERADD = 1)

The first 5 bytes represent the serial number of the VGA microdisplay. The following 48 bytes contain sequential data values that can be used to write to the microdisplay's internal registers starting with register address, "00h", to "2Fh".

Addresses 35h through 5Fh, and addresses 74h through 77h contain factory data not required for operation of the display. This data should not be overwritten.

Addresses beyond 78h are blank.

NOTE: The EEPROM is not write-protected and care should be taken not to activate the Write Mode. The values highlighted in gray are measured at the factory and are specific to each individual device.

| Memory Addr (hex) | VGA OLED Microdisplay |
|----------------------|-----------------------|
| 0 | Serial Char #0 |
| 1 | Serial Char #1 |
| 2 | Serial Char #2 |
| 3 | Serial Char #3 |
| 4 | Serial Char #4 |
| 5 | Data #0 / STAT |
| 6 | Data #1 / VINMODE |
| 7 | Data #2 / DISPMODE |
| 8 | Data #3 / TOPPOS |
| 9 | Data #4 / BOTPOS |
| A | Data #5 ROWRESET |
| B | Data #6 / RAMPCTL |
| C | Data #7 / RAMPCM |
| D | Data #8 /VDACMX |
| E | Data #9 / BIASN |
| F | Data #10 / GAMMASET |
| 10 | Data #11 / VCOMMODE |
| 11 | Data #12 / VCOMCTL |
| 12 | Data #13 / VGMAX |
| 13 | Data #14 / VCOM |
| 14 | Data #15 / IDRF |
| 15 | Data #16 / DIMCTL |
| 16 | Data #17 / TREFDIV |
| 17 | Data #18 / TEMPOFF |
| 18 | Data #19 / TUPDATE |
| 19 | Data #20 / TEMPOUT |
| 1A | Data #21 / ANGPWRDN |
| 1B | Data #22 / SYSPWRDN |
| 1C | Data #23 / TPMODE |
| 1D | Data #24 / TPLINWTH |
| 1E | Data #25 / TPCOLSP |
| 1F | Data #26 / TPROWSP |
| 20 | Data #27 / TPCOLOR |

| | |
|-----------|--------------------|
| 21 | Data #28 / DIGTEST |
| 22 | Data #46 / PUCTRL |
| 23 | Data #47 / HIDDEN |
| 24 | Reserved |
| 25 | Reserved |
| 26 | Reserved |
| 27 | Reserved |
| 28 | Reserved |
| 29 | Reserved |
| 2A | Reserved |
| 2B | Reserved |
| 2C | Reserved |
| 2D | Reserved |
| 2E | Reserved |
| 2F | Reserved |
| 30 | Reserved |
| 31 | Reserved |
| 32 | Reserved |
| 33 | Reserved |
| 34 | Reserved |
| 35 | Reserved |
| 36 | Reserved |
| 37 | Reserved |
| 38 | Reserved |
| 39 | Reserved |
| 3A | Reserved |
| 3B | Reserved |
| 3C | Reserved |
| 3D | Reserved |
| 3E | Reserved |
| 3F | Reserved |
| 40 | Reserved |
| 41 | Reserved |
| 42 | Reserved |
| 43 | Reserved |
| 44 | Reserved |
| 45 | Reserved |
| 46 | Reserved |
| 47 | Reserved |
| 48 | Reserved |
| 49 | Reserved |

| | |
|-----------|-----------|
| 4A | Reserved |
| 4B | Reserved |
| 4C | Reserved |
| 4D | Reserved |
| 4E | Reserved |
| 4F | GMMA00_HI |
| 50 | GMMA00_LO |
| 51 | GMMA01_HI |
| 52 | GMMA01_LO |
| 53 | GMMA02_HI |
| 54 | GMMA02_LO |
| 55 | GMMA03_HI |
| 56 | GMMA03_LO |
| 57 | GMMA04_HI |
| 58 | GMMA04_LO |
| 59 | GMMA05_HI |
| 5A | GMMA05_LO |
| 5B | GMMA06_HI |
| 5C | GMMA06_LO |
| 5D | GMMA07_HI |
| 5E | GMMA07_LO |
| 5F | GMMA08_HI |
| 60 | GMMA08_LO |
| 61 | GMMA09_HI |
| 62 | GMMA09_LO |
| 63 | Reserved |
| 64 | Reserved |
| 65 | Reserved |
| 66 | Reserved |