SVGA+ Rev2 SERIES

852 X 600
ACTIVE MATRIX OLED MICRODISPLAY

DATASHEET
Revision 13

For Part Numbers:

EMA-100080
EMA-100100

eMagin

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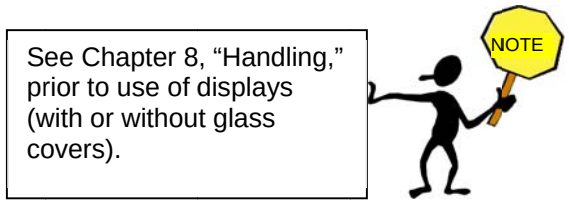
This document describes a low power analog input, color 852 x 600 active matrix organic light emitting diode (OLED) microdisplay with on-chip drivers and interface, intended for use as VESA, SMPTE-170M (monochrome only), or entertainment compatible monitor.

1. INTRODUCTION

The SVGA+ Rev2 OLED Microdisplay has a resolution of 852 x 3 x 600 pixels and was dubbed "SVGA+"((Super Video Graphics Array plus) because they have 52 more display columns than a standard SVGA display. This design permits users to run either (1) standard SVGA (800 x 600 pixels) to interface to the analog output of many portable computers or (2) 852 x 480, using all the data available from a DVD player in a 16:9 wide screen entertainment format. The SVGA+ can be made as a full-color or monochrome microdisplay primarily for high-performance and large-view consumer OEM products such as games, video/data head-wearable displays, digital cameras, video cameras and other portable electronics applications. The display also has an internal NTSC and Pal-CCIR monochrome video decoder suitable for low power night vision systems. This product is designed to interface with most portable personal computers.

As of early 2003, the standard display configuration included a glass cover over the active display area. Prior to March 2004 some display part numbers included a "G" suffix in the part number to designate the glass cover. Effective March 2004 displays shipped without glass will be designated with a "NG" suffix in the part number whereas part numbers with no suffix will designate glass covers.



This specification applies to the following SVGA+ Series OLED microdisplay models:

Color:	EMA-100080
White monochrome:	EMA-100100

NOTE: Please refer to the Defect Criteria Document I03-1000044 for specifics on Defect types

2. GENERAL CHARACTERISTICS

TABLE 2-1. GENERAL CHARACTERISTICS

Parameter	Specification[1]
Format	852 (x3) x 600 pixels
Color Pixel Aspect Ratio	Square
Color Pixel Pitch	15 µm
Color Pixel Arrangement	R, G, B Vertical Stripe
Viewing Area	12.78 x 9 mm
Mechanical Envelope	19.78 x 15.2 x 5 mm
Weight	1.8 grams
Gray Levels	Up to 256 per primary color
Uniformity	> 85% (2)
Contrast Ratio	≥100:1 Intrinsic (Measured per VESA FPDM Standard)
White Luminance Maximum	≥ 70 cd/m^2 (front luminance), SVGA 60Hz VESA mode
Video Inputs R, G, B Inputs Monochrome Input	 0 to 0.7 V, compatible with VESA VSIS standard 0 to 1.0 V, compatible with SMTPE-170M
Video Signal Bandwidth	56 MHz maximum (VESA mode), up to 85Hz frame rate 13 MHz minimum (SMPTE-170 mode), 30 Hz frame rate
Control & Serial Interface	Digital 3.3 V CMOS
Power Interface	
Logic/Analog Supply (Vdd) Van Vcommon	3.3 Volts DC @ 50 mA maximum 4.0 Volts DC @ 50 mA maximum -3.0 Volts DC @ 50 mA maximum
Operating Ambient Temperature*	-40°C to +65°C
Storage Temperature	-55°C to +90°
Humidity	85%RH non-condensing

Note 1: The above data represents consumer and commercial performance specifications, measured at 20°C. Performance will vary at temperatures above or below 20°C. Operation may be possible outside this temperature ranges, especially for short term use, but such use is considered outside of the basic commercial specification range. For additional information about special operating conditions and methods of test, contact eMagin Technical Support.

Note 2: At 100% of gray level brightness and 60 Cd/m^2 luminance. Luminance uniformity measured between the nominal values of five 1000 pixel zones located in the four extreme corners and the center zone of display.

3. FUNCTIONAL OVERVIEW

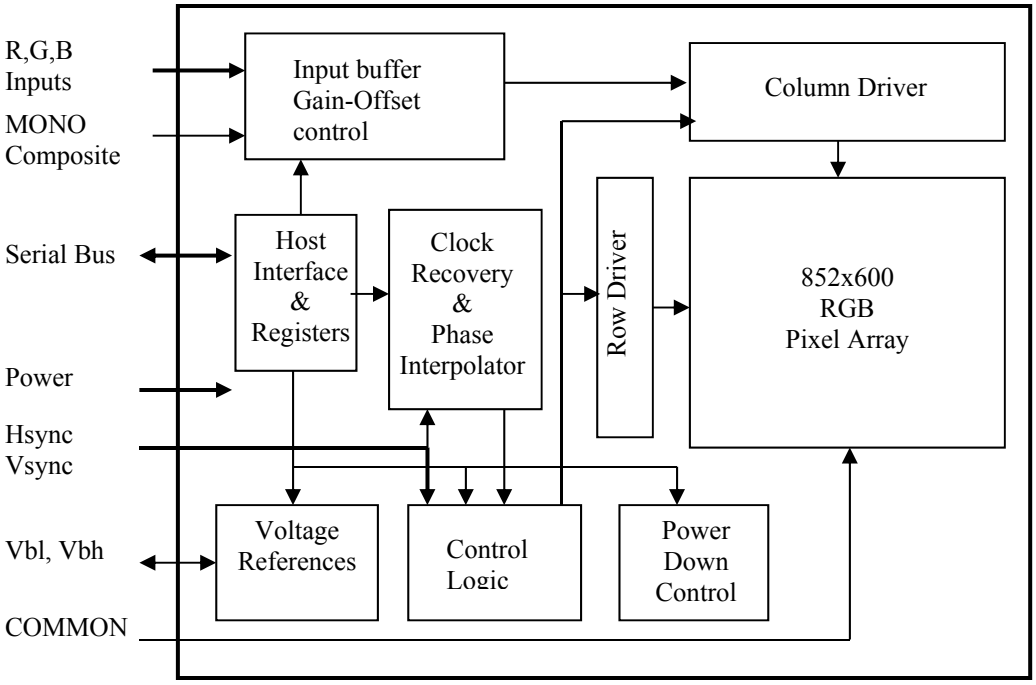


Figure 3-1. Microdisplay functional block diagram

Four (4) analog video inputs are provided: Red, Green, Blue, and Composite Monochrome.

The R, G, B input signals are dc-coupled analog signals with external vertical and horizontal synchronization signals, compatible with the VESA VSIS standard.

The integrated circuit provides for progressive scan color and monochrome modes using the three primary color inputs (R, G, and B).

A dedicated monochrome composite video input (MONO), compatible with the SMPTE-170M standard is provided for monochrome-only interlaced video sources.

In the primary monochrome mode, the input R, G, B signals are internally converted to a monochromatic white signal and applied to all three data channels simultaneously. The secondary monochrome mode uses the dedicated interlaced composite video monochrome input.

In either monochrome mode, the input data is applied equally to the three sub-pixels of each color group. These modes are meant for microdisplays delivered without color filters. The circuit includes a synchronization processing function that extracts the synchronization signals and restores the input signal dc level.

In the color mode, each color input data is delivered in a raster format and fed to an input buffer and a set of sample and hold stages connected in parallel to the input.

The output of the sample and hold (SAH) circuits is applied to the array on a line by line basis during a typical horizontal period. At each pixel cell resides a storage element (capacitor) which is used to control a current source. Gray scale is achieved by generating different current levels through the pixel cell driver circuit. The array is addressed one row at a time as are conventional flat panel displays.

Internal voltage references can be overridden by external inputs to provide a wide-range dimming capability.

The SVGA+ microdisplay has built-in settings for the following video formats:

TABLE 3-1. SVGA+ MICRODISPLAY VIDEO FORMATS

Format (columns x rows)	Name	Input Mode	Output (Display) Mode
640 x 480 Color	VGA	Progressive Scan	Progressive Scan
800 x 600 Color	SVGA	Progressive Scan	Progressive Scan
640 x 480 Monochrome	SMPTE-170M	Interlaced	Interlaced Scan
640 x 480 Monochrome	SMPTE-170M	Interlaced	Pseudo Interlaced Scan
800 x 600 Monochrome	PAL[3]	Interlaced	Interlaced Scan
800x 600 Monochrome	PAL[3]	Interlaced	Pseudo Interlaced Scan
852 x 480 Color	16:9 Format	Progressive Scan	Progressive Scan
852 x 600 Color [4]	Zoom	Progressive Scan	Progressive Scan

NOTES:
1: All progressive scan input modes should use the R, G, B video inputs. All interlaced input modes should use the MONO composite video input. However, all progressive scan color modes are available in the primary monochrome which can be activated through the registers. Other modes are also available..
2: A pseudo-interlaced scan is equivalent to a line-doubling scan during which two adjacent rows are enabled at the same time. A one-row offset occurs every even field.
3: 800 x 600 Monochrome modes are compatible with all forms of PAL/CCIR except for PAL M. PAL M uses 525 lines, thus 640 x 480 Monochrome modes should be used.
4: The Zoom mode is the power-on default operating mode of the microdisplay.

Selection between the non-interlaced and interlaced modes is done through a register set via the on-chip serial interface. The power-up default is a non-interlaced Zoom 60Hz mode.

The serial interface also provides for user adjustments such as contrast, brightness, PLL parameters, display orientation (an externally hardwired control is also provided).

Standard VESA analog video modes do not carry the video clock, which has to be regenerated on chip. A clock recovery circuit based on a digital phase locked loop circuit provides a recovered pixel clock. The PLL has default power-on settings, which can be overridden via the serial interface.

An external video clock input (VCLK) is also available and is enabled/disabled via the serial interface. Default power-up mode is VCLK input disabled.

4. INPUT / OUTPUT DESCRIPTION

Connector Part Number: Hirose DF12D (3.0)-30DP-0.5V

TABLE 4-1. INPUT-OUTPUT DESCRIPTION

Pin #	Name	Type	Description
1	VDD	Power	Power input for the analog and logic circuits 3.3V nominal
2	/RESET	I	System Reset Input (active low). Used to asynchronously reset the entire microdisplay. 100 µs minimum active.
3	SCL	I	Clock port for the serial interface. 400 KHz Max.
4	SDA	I/O	Data port for the serial interface. Open collector output with 2.2K on-board pull-up resistor
5	PWM	O	Logic output. Reserved for test.
6	L/R	I	Left/Right logic input. Used to configure the starting pixel position (left or right)
7	U/D	I	Up/Down logic input. Used to configure the starting row position (top or bottom)
8	SERADD	I	Serial Interface LSB address bit. Must be connected.
9	VAN	Power	Input power for Pixel Array (4.0 VDC nominal).
10	COMMON	Power	Common display terminal. (- 3.0 VDC nominal).
11	GND	Power	Microdisplay power return terminal
12	VBLACK	I/O	Internal Reference Voltage Monitor Output / External Input
13	VBH	I/O	Internal Reference Voltage Monitor Output / External Input
14	VBL	I/O	Internal Reference Voltage Monitor Output /External Input
15	N/C	Open	Not Used
16	N/C	Open	Not Used
17	GND	Power	IC power return terminal
18	RED	I	Analog video signal inputs. 0 to 0.7 V peak to peak.
19	GND	Power	IC power return terminal
20	GREEN	I	Analog video signal inputs. 0 to 0.7 V peak to peak
21	GND	Power	IC power return terminal
22	BLUE	I	Analog video signal inputs. 0 to 0.7 V peak to peak
23	GND	Power	IC power return terminal
24	MONO	I	Composite Video input. 1.0 V peak to peak nominal.
25	VS	I	Vertical Sync logic input. TTL level. Used with non-composite video input
26	HS	I	Horizontal Sync logic input used with non-composite video input. TTL level.
27	VCLK	I	Video data input clock (logic input). Used when the internal clock recovery circuit is disabled. TTL level.
28	N/C	Open	Not Used
29	N/C	Open	Not Used
30	N/C	Open	Not Used

5. ELECTRICAL CHARACTERISTICS

TABLE 5-1. ABSOLUTE MAXIMUM RATINGS

Parameter		Min	Typ.	Max.	Unit
VDD	Front End Power Supply	-0.3		4.6	VDC
VAN	Array Power Supply	-0.3		4.6	VDC
Vcommon	Common electrode bias	-5		0	VDC
Vbl	External Reference	0	2	Van	VDC
Vbh	External Reference	0	2.2	Van	VDC
Vblack	External Black Reference	0	3.6	Van	VDC
VI	Input Voltage Range	-0.3		VDD+0.3	VDC
VO	Output Voltage Range	-0.3		VDD+0.3	VDC
Tst	Storage Temperature	-55		+90	°C
Tj	Junction Temperature	-25		+125	°C
Ilu	Latch up current			+100	MA
Vesd	Electrostatic Discharge – Human Body Model			±2000	V

Stresses at or above those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the following tables is not implied. Exposure to absolute maximum rated temperatures or voltages in the chart below for extended periods may affect device reliability. Prolonged exposure to high temperatures will shorten the luminance half-life. Protection diodes are suggested between Vcommon and ground to protect against power supply spikes.

TABLE 5-2. RECOMMENDED OPERATING CONDITIONS

Parameter		Min	Typ.	Max.	Unit
VDD	Front End Power Supply	3.0	3.3	3.6	VDC
VAN	Array Power Supply	4.0	4.0	4.2	VDC
Vcommon	Common electrode bias	-4	-3.0	0	VDC
Vbl	External Reference	1.6	2.000	2.2	VDC
Vbh	External Reference	1.800	2.218	2.400	VDC
Vblack	External Black Reference	3.4	3.6	3.8	VDC
Tst	Storage Temperature	-55		+90	°C
Ta*	Ambient Operating Temp.	-40	+25	+65	°C
PD	Power Dissipation			450	mW

*Note: The above data represents commercial performance specifications, measured at 20°C. Performance will vary at temperatures above or below 20°C. Operation at higher or lower temperatures is possible but may require compensation via biasing to maintain the 20°C optimum performance. Half-life is reduced at high temperatures. Operation may be possible outside the temperature ranges specified in Table 5-2, especially for short term use, but such use is considered outside the basic specification range. Operation outside the recommended operating conditions will void any warranty.

The consumer OEM specification for acceptable operating and storage temperature range is different from the above chart; refer to the SVGA-3D specifications for this parameter.

Contact eMagin customer service regarding potential use of the display under other conditions. Warranties for use under other operating conditions require formal written documentation specifically extending the warranty to these conditions. Statement of potential acceptable use under alternate conditions by company personnel does not constitute a warranty extension.

TABLE 5-3. DC CHARACTERISTICS DC CHARACTERISTICS

Ta = 20°C, GND = 0V, VDD = +3.3V, VAN = +4V, Vcommon =-3.0

Parameter		Min	Typ.	Max.	Unit
Vil	Digital input low level	GND-0.3		1	VDC
Vih	Digital input high level	2.0		VDD+ 0.3	VDC
Vol	Digital output low level			0.5	VDC
Voh	Digital output high level	2.4			VDC
Ivbh, Ivbl [3]	External Reference Current	-10	0.18	0.3	mA
Ivblack	External Black Reference Current		0	0.05	mA
V MONO [1]	MONO Analog input dc level	0		1.0	VDC
V R,G,B [2]	VESA Inputs signal level	0		0.7	VDC
Pd Van	Average Van Power Dissipation (SVGA Mode 60 Hz refresh rate)		60	150	mW
Pd VDD	Average VDD Power Dissipation (SVGA Mode 60 Hz refresh rate)		140	180	mW
Pd VCOM	Average VCOMMON Power Dissipation (@ -3.0V)		50	150	mW

Notes:
1: The RED, GREEN and BLUE inputs are CMOS inputs. No termination other than those required by the driving source and cable characteristics are required
2: The MONO channel includes a dc restore circuit. A non-polarized ac coupling capacitor is required for proper operation.
3: When using external voltage references for Vbh and Vbl, the SVGA+ microdisplay will output up to 11 mA at each pin (Vbh and Vbl)

TABLE 5-4. AC CHARACTERISTICS

Ta = 20°C, GND = 0 V, VDD= +3.3V, Van = +4.0V, VCOMMON =-3.0

Symbol	Parameter	Min	Typ.	Max.	Unit
Fvclk	Video Clock Frequency	10	-	56.25	MHz
Ths	Horizontal Sync frequency	15.7		53	KHz
Thsw	Hsync Pulse Width	2			Tclk
Tvs	Vertical Sync Frequency[1]	30		85	Hz
Tvsw	Vsnc Pulse Width	2			Tclk
Trst	Reset Pulse Width	100		-	µs
Cpwm	PWM Output Load		4	8	pF
Cav	Analog input capacitance	5		8	Pf

Note 1: Maximum refresh rate for SVGA mode is 85 Hz. For interlaced mode the frame rate may be as low as 30 Hz (SMPTE Modes)

Analog R, G, B Input Characteristics

5.1.1. Input Characteristics

(per VESA VSIS rev 1.0)

TABLE 5-5. INPUT CHARACTERISTICS

Parameter	Value	Comment
Max Luminance (1)	0.700 Volts - 0.035 Volts/ +0.07 Volts	
Min Luminance (1)	0.000 Volts	
Video Channel Rise/Fall Time Max	50% of minimum pixel clock period	
Video Channel Rise/Fall Time Min	20 % of minimum pixel clock period	
Settling Time Max	30% of minimum pixel clock period	
Monotonic	Yes	
Resolution	1 LSB	
Integral Linearity Error	+/- 1 LSB	
Differential Linearity Error	+/- 1 LSB	
Video Channel to Video Channel Mismatch	6% of any output voltage over the full voltage range	
Noise injection ratio	0.5 % of Max Luminance Voltage	All Sources DC to Max Pixel Frequency
Video Channel to Video Channel Output Skew	25% of minimum pixel clock period	
Overshoot/ Undershoot	+/-12% of step function voltage level over the full voltage range	1.5 X the rise time duration

(1) With respect to GND.

6. OPTICAL CHARACTERISTICS

TABLE 6-1. EMA-100080 COLOR MICRODISPLAY OPTICAL CHARACTERISTICS

Conditions: Ta = +20°C, GND = 0 V, VDD= +3.3V, Van = +4.0V, Vcommon =-3.0

Symbol	Parameter	Min	Typ.	Max.	Unit
L	Front Luminance	0.1	100	200	Cd/m^2
CR	White to Black Contrast Ratio	100:1	-	-	
U	Area Uniformity	80%	90%	100%	
CIE White	X	0.27	0.32	0.37	
	Y	0.28	0.35	0.38	
Gray Levels	Ng	64	256	-	Levels
Refresh Rate[1]	Progressive scan mode	40	-	85	Hz
	Interlaced scan mode	30	-	85	Hz
Pixel Cell	Sub Pixel Width Pitch		5		µm
	Sub Pixel Height Pitch		15		µm
Fill Factor	% Emissive Area vs. total subpixel area	59	62	65	%

Note 1: Specification refers to value producing no visible image flicker

TABLE 6-2. EMA-100100 MONOCHROME WHITE MICRODISPLAY OPTICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ.	Max.	Unit
L	Front Luminance	0.1	540	820	Cd/m^2
CR	White to Black Contrast Ratio	100:1	-	-	
U	Area Uniformity	80%	90%	100%	
CIE	X	0.27	0.32	0.37	
	Y	0.295	0.345	0.395	
Gray Levels	Ng	64	256	-	Levels
Refresh Rate[1]	Progressive scan mode	40	-	85	Hz
	Interlaced scan mode	30	-	85	Hz
Pixel Cell	Sub Pixel Width Pitch		5		µm
	Sub Pixel Height Pitch		15		µm
Fill Factor	% Emissive Area vs. total subpixel area	59	62	65	%

Note 1: Specification refers to value producing no visible image flicker

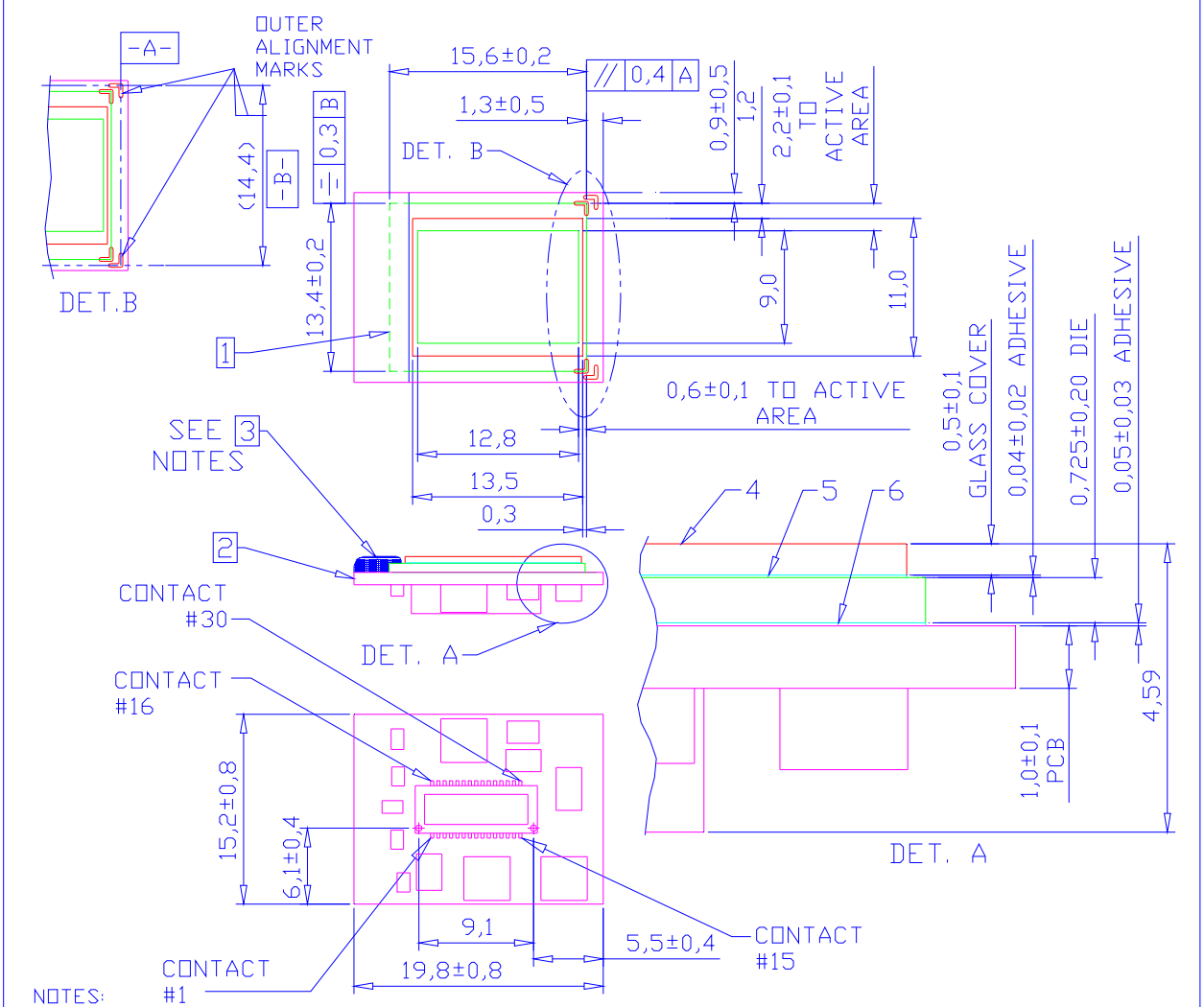
Optical characteristics are measured in accordance with the VESA Flat Panel Display Measurement Standard, Rev 1.0 (A copy of the standard is available at the VESA website: www.vesa.org).

Measurement Conditions

Luminance, contrast and chromaticity measurements are performed in a dark ambient environment at room temperature, on a dedicated automated test bench. The reference used for the luminance measurement is the OLED current density, set to 20 mA/cm2. In order to account for possible leakage effects, the OLED current, measured at the Vcommon terminal, is first measured when the video input has been set to black. The Vcommon current is then recorded (dark current) and the video input is set to white (maximum video input level). The Vcommon current is then adjusted to add exactly 20 mA/cm2 to the dark current. The "white" luminance is then measured, as well as the color coordinates. The contrast is then obtained by taking a luminance measurement with the video inputs set to black without adjusting any other parameter.

7. MECHANICAL CHARACTERISTICS

RevNo	Revision note	Date	Signature	Checked
01	Increase Encapsulant coverage around display edges	11.13.2007		
02	Encapsulant coverage changed, 13.5 glass lid was 14.0	10.21.2008	J.K.	O.P.



NOTES:

1.THE HEIGHT OF THE ENCAPSULATION MUST BE FLUSH WITH OR LOWER THAN THE HEIGHT OF THE GLASS COVER.

2. NO CONTACT BETWEEN ENCAPSULATION AND GLASS LID.

ALL DIM. IN MM

ACCURACY X.X±0,3 UNLESS MARKED OTHERWISE

PROJECTION

6	1	DIE ATTACH ADHESIVE	
5	1	GLASS COVER ADHESIVE	
4	1	GLASS COVER	C05-500115-01
3	AS REQ.	WIREBOND ENCAPSULANT	
2	1	P.C. BOARD ASS'Y	EMA-100068
1	1	MICRODISPLAY	EMA-100034

Figure 7-1. Mechanical Characteristics

Connector J1

Manufacturer:	Hirose
Manufacturer Part Number:	DF12D (3.0)-30DP-0.5V

Mating Connector Information

Manufacturer:	Hirose
Manufacturer Part Number:	DF12A(3.0)-30DS-0.5V
Weight:	1.9 g (nominal)

Printed Circuit Board Material:	FR4
Printed Circuit Board Tolerances:	± 0.8 mm (both axes)

8. CLEANING HANDLING AND STORAGE RECOMMENDATIONS

8.1 Cleaning:

When cleaning the displays we recommend the use of TECH-SPEC lens cleaner, manufactured by Edmund Optics Inc. and Alpha wipes 1010

8.2 General handling considerations:

- Do not expose the display to strong acids, bases, or solvents.
- Do not expose the display surface to UV or other strong ionizing radiation
- Temperatures in excess of the specified operating and storage range can cause irreversible damage to the display.
- Do not allow sharp objects to contact the exposed regions of the silicon display chip.
- Avoid immersion of the display in any liquid.
- The glass cover slip protects the display surface from most forms of damage and may be cleaned using techniques appropriate for fine lenses.
- Avoid applying force to the glass relative to the display chip in compressive, tensile, and sheer directions.

Fig. 3 Best method of handling the displays

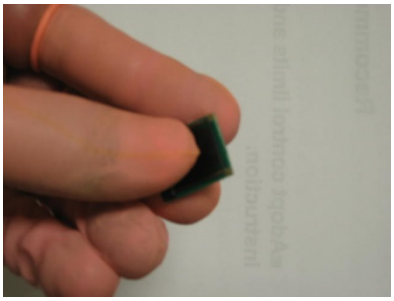


Fig. 4 Avoid this method of display handling

8.3 Static Charge Prevention:

The microdisplay is sensitive to electro-static discharge damage. The following measures are recommended to minimize ESD occurrences:

- When handling the microdisplay, operated under a flow of ionized air to discharge the panel
- Use a conductive wrist strap connected to earth ground via a 10 M-Ohm resistor.
- Wear non-chargeable clothes
- Keep stored displays away from charged materials

8.4 Protection from Dust and Dirt:

It is also recommended that all display handling operations take place in a clean environment. The use of ionized nitrogen gas is the preferred method of removing particles from the surface.

8.5 Short Term Storage:

For short term storage (one to two weeks or less), the displays should be kept in their original container at room ambient and the typical controlled office environment.

8.6 Long Term Storage:

For displays that will be stored for a longer period (a few weeks and up), it is recommended to keep displays stored in a dry environment near or at room ambient (20ºC typically) whenever possible prior to installation into an optical subsystem.

There are several ways to achieve this:
- Dry storage cabinet
- Dry Nitrogen cabinet
- Nitrogen sealed bag
- Vacuum sealed bag with desiccant

9. DETAILED FUNCTIONAL DESCRIPTION

Input Buffer

The Input Buffer assumes DC-coupled RED, GREEN and BLUE analog inputs. The inputs are high impedance CMOS inputs and do not require any special termination.

The MONOCHROME analog input is the output of the Video Sync Processor and consists of a video signal that has been stripped of the synchronization pulses and dc restored to ground. The first stage of the buffer circuit provides for removal of the CRT gamma provided by the host (for use with the MONO input only) as well as a correction to accommodate the internal non-linearities of the data path.

In the primary monochrome mode, the Red, Green and Blue inputs are summed (weighted sum with equal weights) to yield a monochrome white video signal prior to entering the second stage.

The buffer circuit includes gain and offset adjustments controlled via the serial interface. Digital potentiometers are used to adjust the signal characteristics. Each channel includes two registers, one for amplitude (contrast) and one for offset (brightness). Each control has a ± 50% range and defaults to 1 (Gain) and 0 (Offset) at power up.

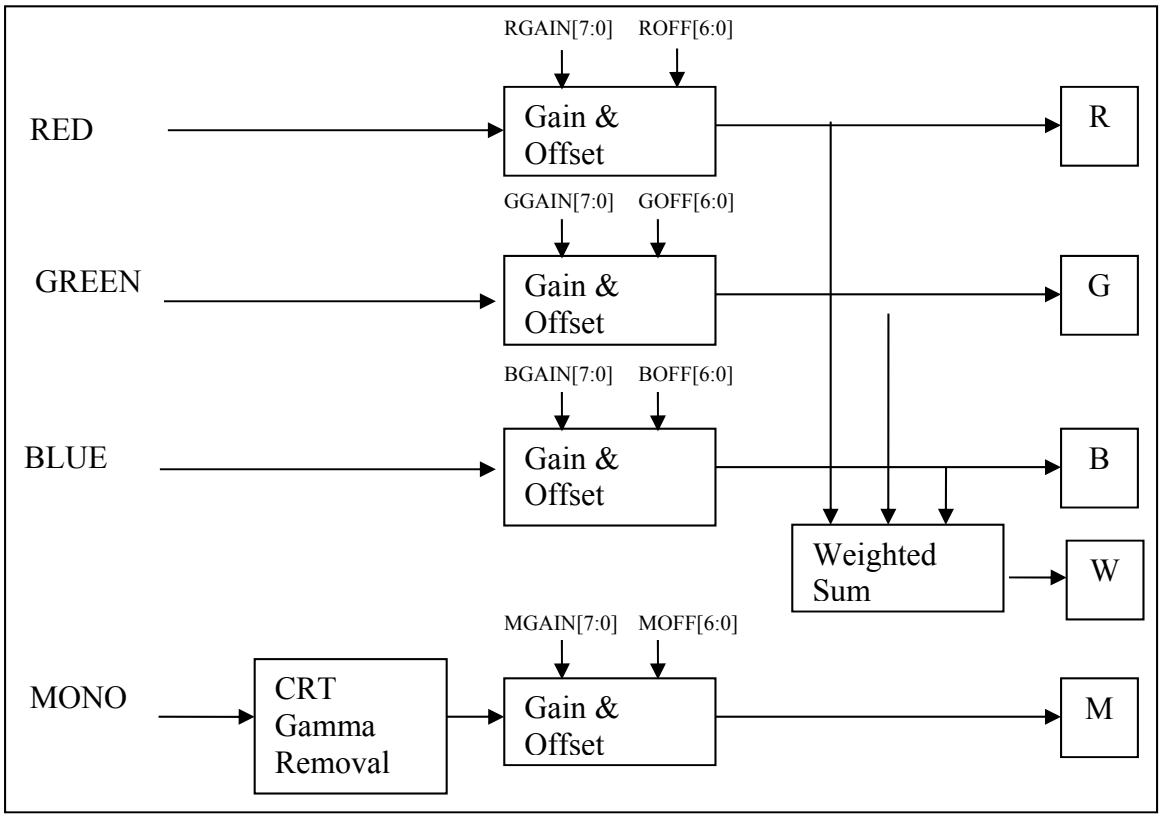


Figure 9-1. Analog Inputs Block Diagram

Following the gain and offset stage, three 3:1 multiplexers channel the selected input (Color, White or Mono) to one of three data channels that are fed to the Data Sampling functional block. Each channel maps into 852 cells per row.

The input selection is controlled by the VMODE register, accessible via the serial interface. The lower two bits, COLSEL1 and COLSEL0, are used.

TABLE 9-1. INPUT MULTIPLEXER SELECTION CONTROLS

COLSEL[1]	COLSEL[0]	MODE	Mux1 Out	Mux2 Out	Mux3 Out
0	0	Color	R	G	B
0	1	White	W	W	W
1	0	Composite	M	M	M
1	1	Color	R	G	B

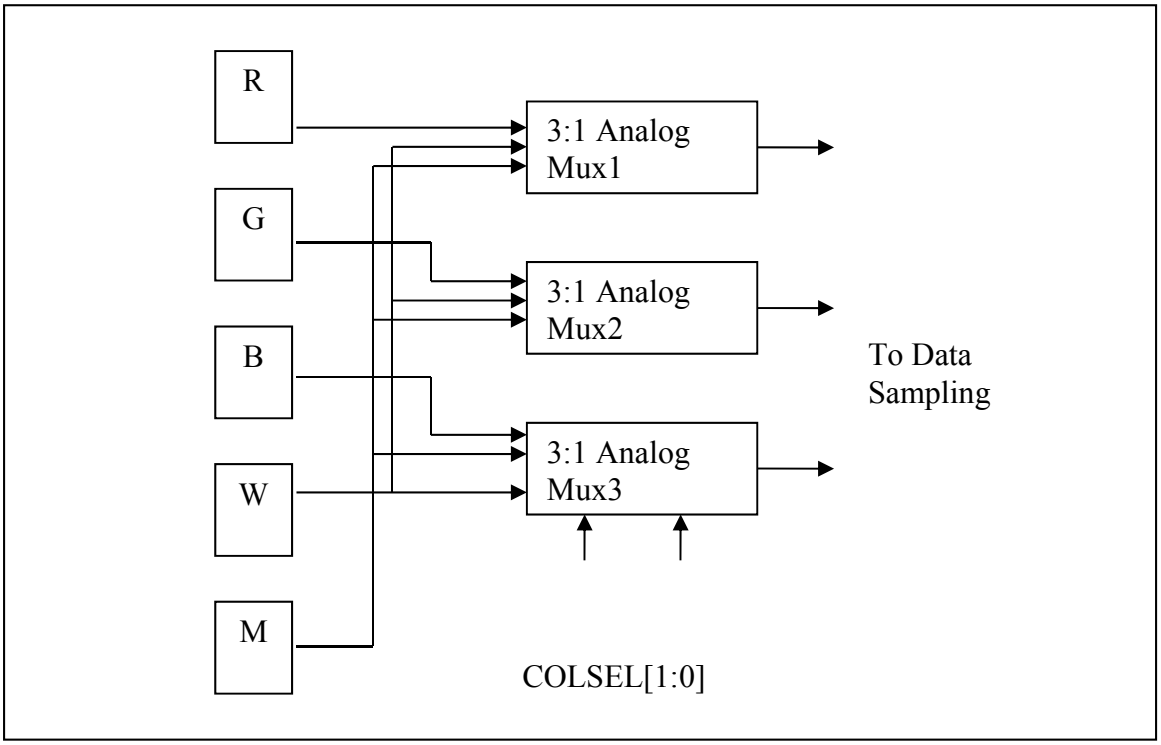


Figure 9-2. Input Multiplexer Block Diagram

Data Sampling

The output of the multiplexers is fed to multiple dual sample and hold stages. The design approach is a pipeline mode where the raster line input data is sampled then held to allow for propagation to the relevant pixel cell, while allowing for the sampling to continue uninterrupted using the second sampling capacitor. The stages are optimized to achieve the best balance between low power (via bandwidth reduction and minimum loading of the buffer) and performance (uniformity, noise and internal propagation delays).

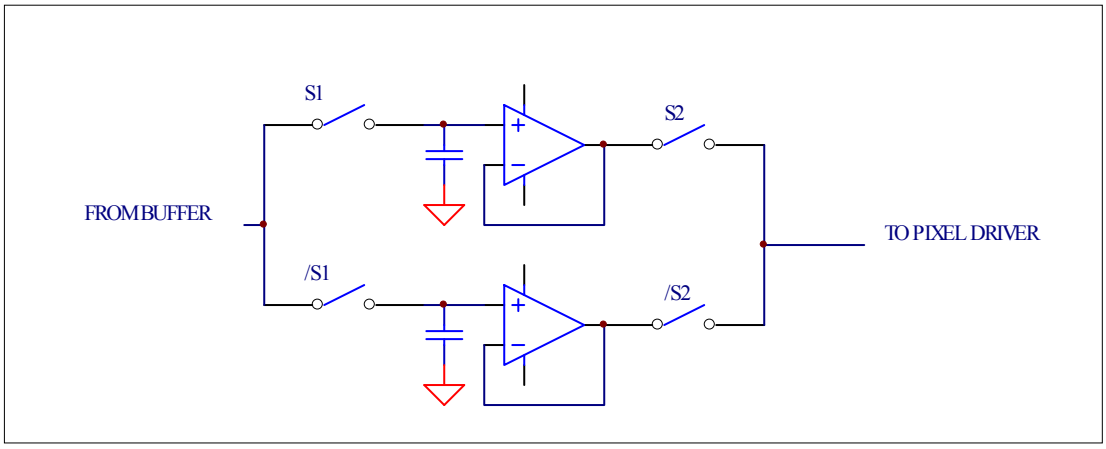


Figure 9-3. Dual Sample & Hold Block Diagram

The analog switches are designed to minimize charge injection and dynamic power dissipation.

The sample and hold amplifier is a unity gain element with low fan out requirements. Its output is fed directly to the pixel driver circuit. The sequence controlling which SAH is being selected is generated by the column sequencer block. This includes start and end of active video sampling.

Pixel Cell

There are 2,556 pixel cells (852 x 3) per active row (600active rows). Each cell is a 5 x 15-micron rectangle, yielding a 15 x 15-micron square color group (RGB).

The pixel cell output stage is a current source configured around a PMOS transistor. The current flows from the VAN power input to the OLED's anode terminal. The OLED is typically represented as a diode. OLEDs generate an amount of light that is proportional to the current density flowing through the device.

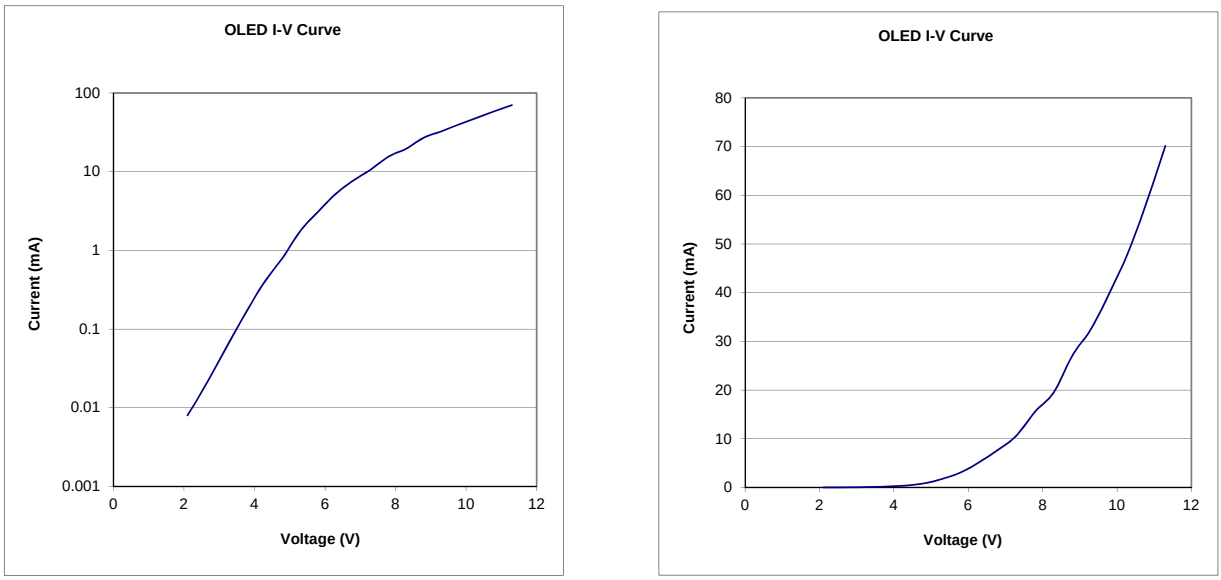


Figure 9-4. OLED I-V Characteristic (Log and Linear scale)

The pixel cell operates at VAN power to maximize the dynamic range of the display technology as well as accommodate its life-dependent voltage characteristic.

The cathodes of all OLED pixels are electrically connected to the COMMON pin via an internal electrode that surrounds the array.

Pixel Driver

The pixel driver block buffers the sampled signal to an output tuned to the array characteristics. There are as many pixel drivers as there are dual SAH stages.

At the beginning of each video line, the pixel driver output is reset to the black level. This will ensure a consistent reference level on the data lines and reduce the impact of potential residual charges.

The Pixel driver is designed around a current source operated in the sub-threshold region in order to output the low current required by the OLED to generate modulated light. The driver works in two phases, a programming phase and a run phase

During the programming phase, which lasts for one row period, the output of the sample and hold charges the pixel storage capacitor with a current approximately 100 times greater than the value needed for light emission. This provides for enough settling time over the specified refresh rate range.

During the run phase, which lasts for one entire frame period minus one row period, the pixel driver output current is scaled down by switching the drive transistor into its sub-threshold operation region. This is achieved by changing the storage capacitor reference level.

This method preserves the dynamic range as well as the linearity of the overall transfer function.

VOLTAGE REFERENCES

Three reference voltage levels are used in the pixel driver circuit: Vblack, Vbl and Vbh. These levels can be generated internally or provided externally.

The power on condition for the reference is the internal reference. This setting can be overridden by powering down the internal references after power-up using register 17h (PDWN) bits 4,5, and 6 (Set to 1 for power down), and register 18h (ATB) bit 7 (Set to 1 to allow use of register 17h). The output impedance of the internal reference generator is high enough that an override is possible even without powering them down.

For applications that require a luminance level adjustment over a large range, or for applications that use two displays and need to have their luminance levels closely matched, the use of external references for Vbl and Vbh is recommended.

Care must be taken when designing an external voltage reference circuit for Vbl and Vbh. There is a residual output current at the Vbh and Vbl pins, even after powering down the references. This current can reach 10 mA depending on the value of Vbl and Vbh. An application schematic is provided below that can serve as a basis for a production design.

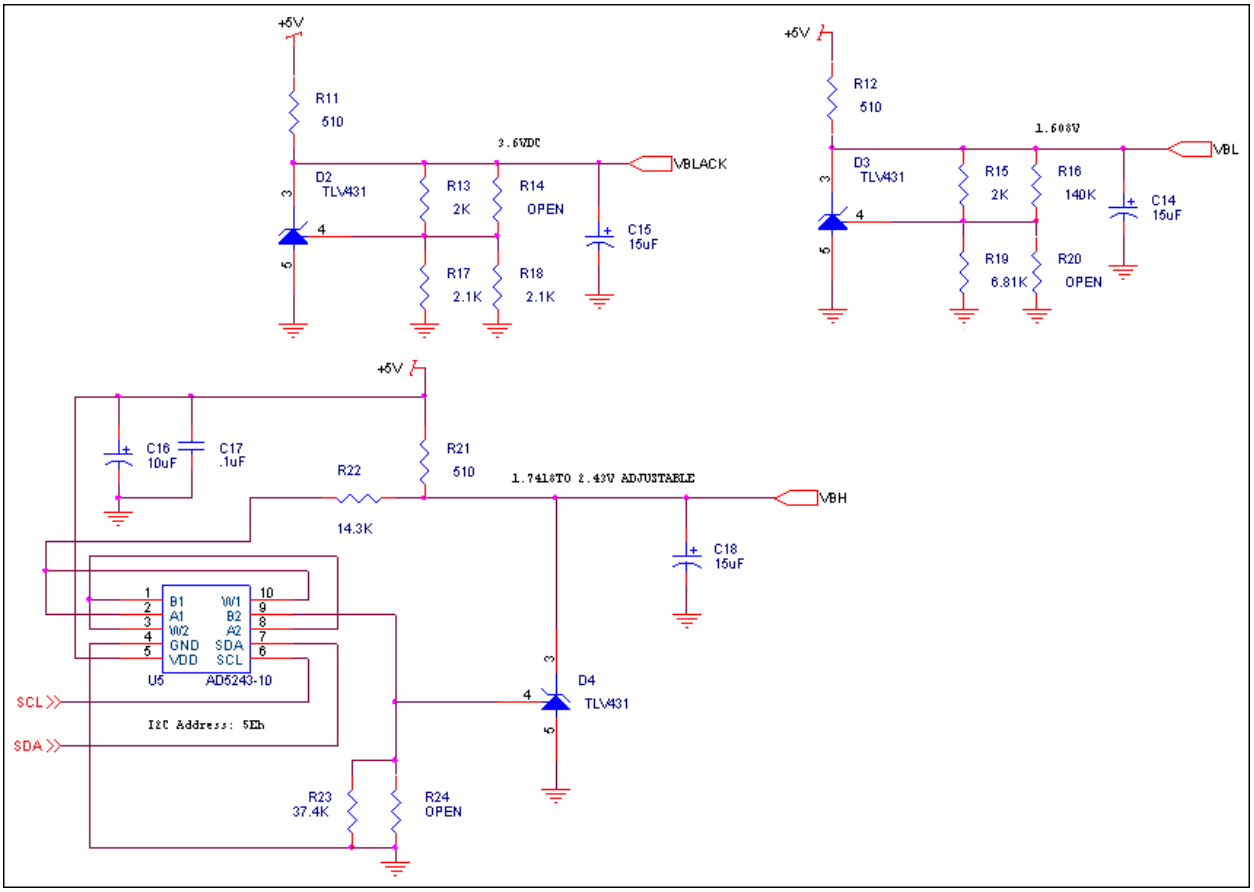


Figure 9-5. Sample Circuit Designs Using External References

Vbl is the reference level used during the programming phase of the pixel driver operation. During this phase the pixel driver is programmed at a higher current value than needed for image restitution. This is done for settling time reasons. This level is active one row per frame for each pixel driver.

Vbh is the reference level used during the light emission phase of the pixel driver operation which lasts most of the video frame. Vbh switches the pixel driver current range down by roughly 100 times in order to bring it to the typical operating levels required by the OLED.
Vbh operates typically at 200 mV above Vbl.
Varying Vbh causes the current through the OLED to change and thus the luminance to change. Since this is a global input, it affects the entire display and therefore can be used for dimming control. The

relationship between Vbh and the luminance is exponential. The dimming range can be over 1000:1 over 200 mV. One consequence of this relationship is the high sensitivity to Vbh. A few millivolts will yield a large luminance variation.
Note that bringing Vbh less than 100 mV above Vbl will result in a washed out display with no modulation as well as a high luminance level that will accelerate the display aging.

The graph below illustrates the luminance response as a function of Vbh for a color microdisplay. For this measurement, Vbl = 2.0V

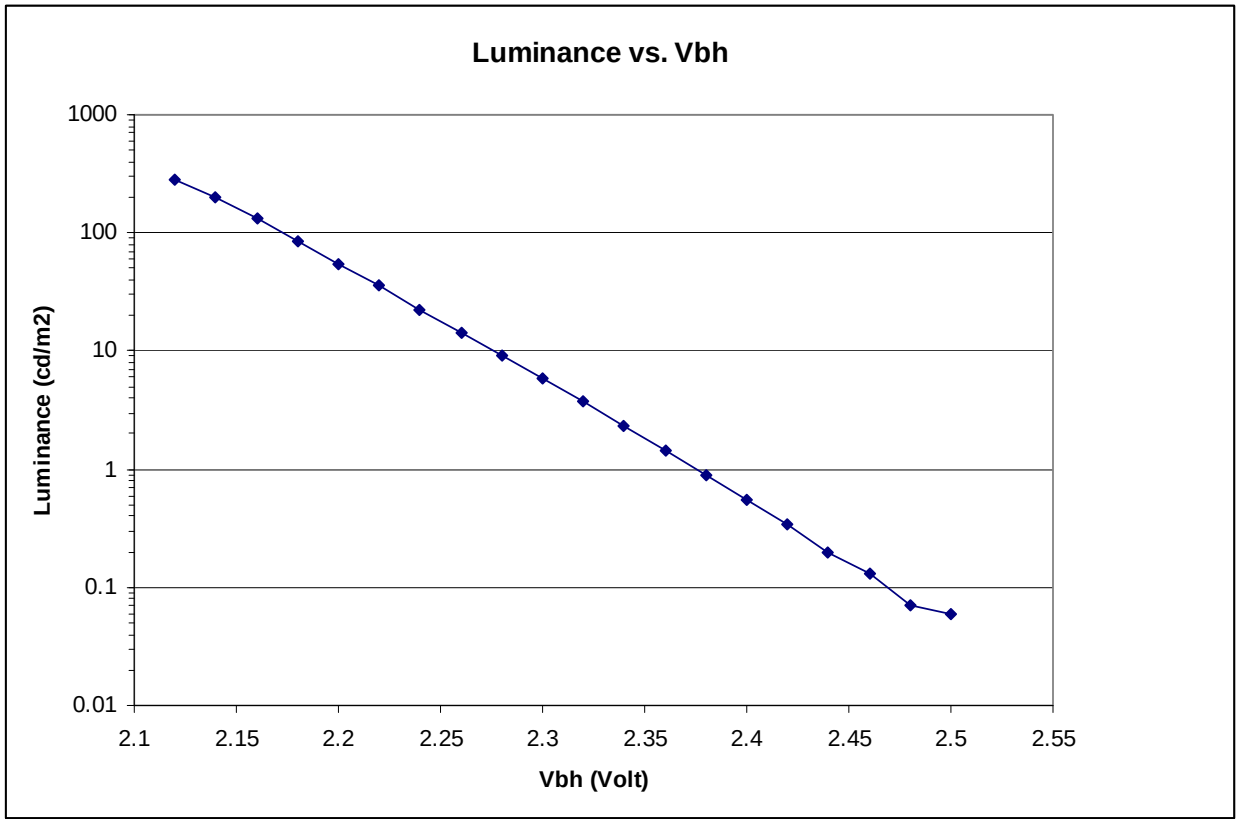


Figure 9-6. Luminance as a Function of Vbh

The internal voltage references use a bandgap circuit to set the levels. The bandgap accuracy is about 3%. Given the exponential dependence of the luminance on Vbh, large luminance variations from die to die are to be expected. As a result, applications that require fixed luminance (such as binocular setups) are better off using externally generated voltage references. With such an approach the mismatch between any two displays is unlikely to exceed 10%.

Vblack is a reference level used to reset the pixel driver to the black level at the beginning of each line. Using an externally generated voltage level can improve the display contrast ratio significantly, albeit with a higher variability from display to display. Adjusting Vblack only affects the black level (0V video input) and has no impact on the maximum luminance. The internal Vblack reference circuit output is nominally 3.45V. An optimum value for an externally generated Vblack is 3.60 V. The reference is a dc level reference that requires very little current (less than 50 micro Amperes).

The graph below shows the typical contrast ratio (dark ambient measurement) as a function of Vblack for the SVGA+ color microdisplay. Two curves were taken for two different values of Vbl for information purposes.
For reference when Vbl = 1.6V, Vbh= 1.805V. When Vbl = 2.0V, Vbh = 2.218V

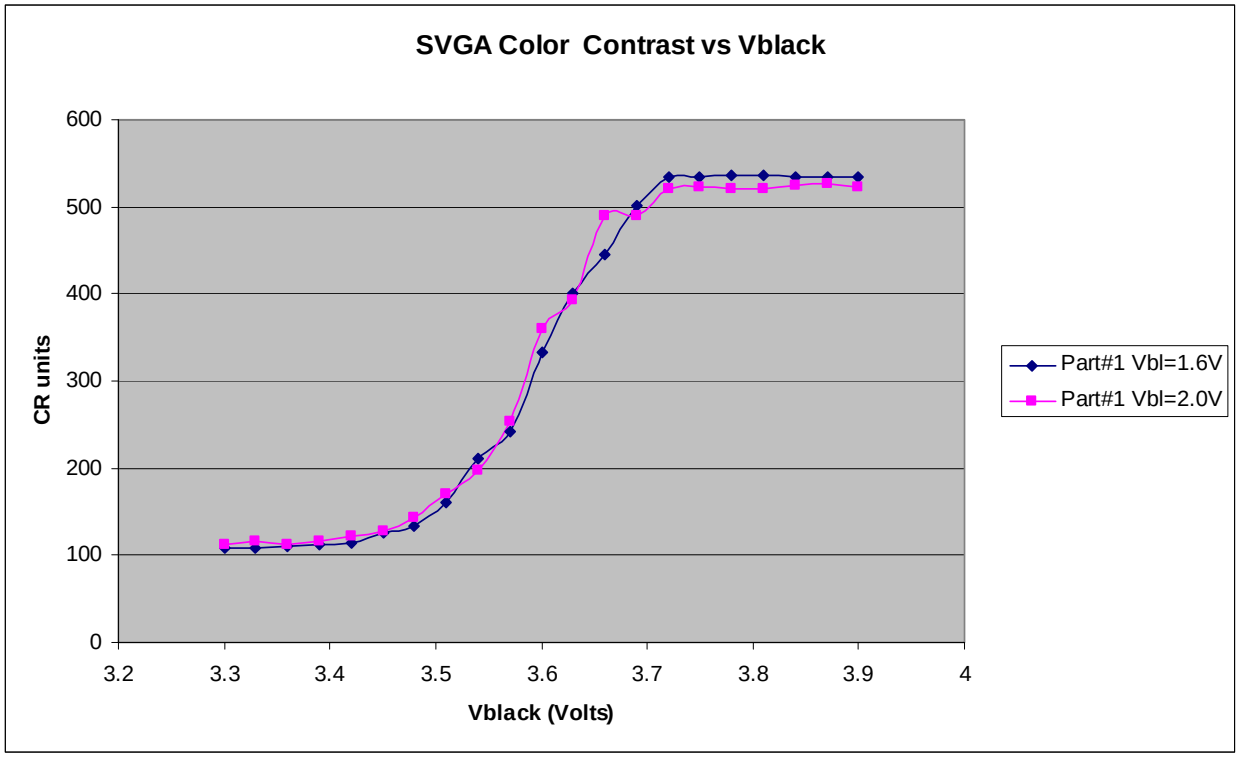


Figure 9-7. Typical Contrast Ratio as a Function of Vblack

Vertical Sequencer and Row Driver

The row driver is designed around a 600-stage shift register. For nomenclature and reference purposes, Row # 1 is set arbitrarily to be the top row when viewing the display with the I/O pads on the left.

The shift register is bi-directional. The direction is set by the U/D external input or by bit 5, VSCAN, in the VMODE registers. The priority is set by bit 6, VSCANS of the same register. When VSCANS = 0, the external input has priority. When VSCANS = 1, VSCAN has priority. When U/D = GND or VSCAN = 0, the display is scanned from top to bottom (increasing row number sequence). When U/D = VDD or VSCAN = 1, the display is scanned from bottom to top (decreasing row number sequence).

The table below summarizes the various vertical modes. Interlaced modes are limited to a maximum of 300 and a minimum of 240 active rows per field. The table is provided assuming VSCAN = 0. The reverse direction start and end rows are symmetric with respect to the center of the array.

TABLE 9-2. VERTICAL SEQUENCER CONTROLS

VSEL2	VSEL1	VSEL 0	Vertical Mode
0	0	0	SVGA / Zoom (600 Rows)
0	0	1	VGA / 16:9 (480 Rows)
0	1	0	Interlaced 2 (600 Rows)
0	1	1	Pseudo Interlaced 2 (600 Rows)
1	0	0	Interlaced 1 (480 Rows)
1	0	1	Pseudo Interlaced 1 (480 Rows)
1	1	0	SVGA / Zoom (600 Rows)
1	1	1	SVGA / Zoom (600 Rows)

The vertical sequencer gets inputs from the Sync Processor block and the serial interface. The vertical sync with or without serration pulses (non-interlaced or interlaced/pseudo interlaced mode), the field polarity (for interlaced/pseudo interlaced modes), and the horizontal clock come from the Sync Processor block. Register VSTART is used to determine the start of the vertical active window. In addition, counters are used to sample the horizontal clock and/or the serration pulses. The start of the active vertical window is determined by a match between the output of the counters and the value in the register VSTART. The end of active scan occurs when the shift register runs out. A new vertical start strobe is required to start the shift register again.

For interlaced modes, the odd field maps to the odd rows and the even field maps to the even rows. The field polarity output from the Sync Processor is used in conjunction with the vertical sync signal to control the odd/even rows selection.

The row shift register can be started at various stages, depending on the video mode selected by the user. Selected cells of the shift register have input multiplexers to allow for alternate start/end points. The shift register can also be configured for interlaced and pseudo interlaced scan operations. These settings are determined by the VSEL [2:0] bits in the VMODE register.

In a progressive scan mode, rows are addressed in a sequential manner. In an interlaced scan mode, every other row is addressed in a sequential manner. The polarity of the addressed rows depends on the value of the FIELD bit (internal output of the Sync Processor function). Thus, the first active row may be an odd or even row. The unaddressed rows are left unselected.

In a pseudo-interlaced mode, rows are addressed as pairs, in a sequential manner. Depending on the value of the FIELD bit, the first row of the first pair may be an odd or an even row. Thus, there is a one row vertical offset between odd and even fields. In these modes, all active rows are addressed for each field, except for the first active row of the even field, which is left unselected.

The table below summarizes the row selection and addressing for progressive, interlaced and pseudo interlaced modes.

TABLE 9-3. MICRODISPLAY ROW SEQUENCE

Input Active Row Period Number	Display Row Sequence			
	Progressive Scan	Interlaced Scan (Odd Field)	Pseudo Interlaced Scan Odd Field	Pseudo Interlaced Scan Even Field
1	1	1	1,2	2,4
2	2	3	3,4	3,5
3	3	5	5,6	6,7
4	4	7	7,8	8,9
5	5	9	9,10	10,11

The shift register is reset at the end (or beginning) of each frame. For modes other than SVGA and Interlaced 1, all inactive rows are set to the off state (black) automatically. The shift register is clocked at the line rate to minimize power dissipation (as opposed to being clocked by the video clocked and gated by an enable signal).

Horizontal & Burn-in Sequencers

The horizontal sequencer generates the timing signals needed to control the sample and hold circuit switches. The start and end of the sampling sequence depends on the video mode selected (COLSEL [1:0]).

The start and end of the active video line are centered with respect to the center of the display in order to avoid image miss registration when implementing a bi-ocular headset.

The horizontal sequencer provides for left/right support via the L/R input pin or an internal bit, HSCAN, of the HMODE register. The reference used (L/R or HSCAN) is determined by the value of bit HSCANS (bit 4 of the HMODE register). When HSCANS = 1, HSCAN determines the horizontal shift direction. The power-up default is HSCANS = 0.

Assuming HSCANS = 1, when HSCAN = 0, the image starts at the left side of the display IC. The image is displayed on a line by line basis, starting at the leftmost column of the display window. When HSCAN = 1, the image starts at the right side of the display window.

The HSTART register is used to set the starting point of the active sampling window. HSTART is programmed in units of the pixel clock. The power-up default is set to 84h (132d), which corresponds to the default Zoom @ 60Hz settings.

Bits HSEL [2:0] of register HMODE are used to configure the display format for the horizontal sequencer.

TABLE 9-4. MICRODISPLAY HORIZONTAL MODE CONTROLS

HSEL2	HSEL1	HSEL 0	Horizontal Mode
0	0	0	Interlaced 2 /Pseudo Interlaced 2 (800 Columns)
0	0	1	VGA / Interlaced 1 / Pseudo Interlaced 1 (640 Columns)
0	1	0	SVGA (800 Columns)
0	1	1	Interlaced 2 /Pseudo Interlaced 2 (800 Columns)
1	X	X	16:9 & Zoom 2 (852 Columns)

All starts and ends occur on a color group boundary.

9.1.1. Burn-in compensation Sequencer

For all modes except 16:9 and Zoom modes, the start and end column positions can be shifted by ± 5 columns at a programmable rate to minimize visible pattern burn in when use of the display fixed image is anticipated... This is done to smooth out sharp edges that may arise in graphics mode with fixed patterns such as cursors or icons. A programmable 16-bit counter (HRATE [15:0]) is strobed by the vertical synchronization pulse. When the count terminates the start and end columns are shifted by

one position. When the number of shifts has reached five (5) the direction of shift is reversed, and so on. The compensation mode is selected via the user interface, as is the count.

The default power-up value for HRATE [15:0] is 8000h, which corresponds to a 9 minute per column shift. At 60 Hz, the column shift rate can be adjusted from 0 to 18 minutes.

eMagin does not warranty against fixed pattern burn in effects. It is the customer's responsibility to minimize use of the display with fixed patterns for extended periods. Automatic turn off of the display when not in use is recommended to minimize luminance loss or pattern burn in. The luminance reduction rate increases at high temperatures, so added attention to minimizing fixed pattern use should be taken above 40 ºC.

Should a fixed pattern burn in occur, fixed patterns can typically be mostly erased by running the screen for long periods of time with random motion video (e.g., TV, screen savers, or movies), inverse patterns to the burn-on pattern, or all-white screens. For additional information, please contact eMagin Technical Support.

Clock Recovery

The integrated circuit includes a clock recovery unit based on a phase-locked loop circuit. The PLL's modulus divider is programmed through the serial interface. Its default power-up value is set for a 60Hz SVGA video mode.

The circuit regenerates the pixel clock based on the horizontal synchronization input (line locked system). This signal is generated by the Sync Processor and has been conditioned to provide a short rise/fall time. The on-chip voltage controlled oscillator is fed by the phase detector through an external low pass filter resistor/capacitor combination.

The output of the VCO feeds a programmable post-scaler (divide by 1,2,4,8 and 16) and the feedback divider. A post-scaler is required to ensure compatibility of a single VCO with VGA through SXGA video formats, as well as the interlaced video modes (lower frequency).In addition, a charge pump gain control is provided to match the pump's output to the frequency selected.

The PLL circuit provides for fine phase adjust via a dedicated register (PI2). A programmable delay controls the clock phase with respect to the recovered HSYNC signal. The unit delay is $1/32^{nd}$ of the clock period after the post scaler.

The phase interpolator circuit can be bypassed and powered down by setting the PIBYP bit to 1 in the PI2 register. In this configuration, only four phase selections are possible (0, 90, 180, and 270 degrees).

The IC supports eight VESA standard monitor-timing configurations and up to two interlaced timings:

-VGA 640 x 480 @ 60, 72, 75 & 85 Hz non-interlaced

-SVGA 800 x600 @ 60, 72, 75 & 85 Hz non-interlaced

-Interlaced 480 active lines (240 per field), timing and levels per SMPTE-170M

-Interlaced 600 active lines (300 per field), levels per SMPTE-170M

The Clock recovery circuit can be entirely bypassed and powered down by setting the CLKS bit to GND in the HMODE register. In this mode, the external pin VCLK is used as the source clock for the microdisplay.

Sync Processor

The Sync Processor primary function is to extract the synchronization signals from the composite monochrome video input (MONO) and output the recovered horizontal, vertical, and field polarity signals. In addition, it provides dc restore for the sync-stripped video signal.

For non-interlaced video modes, the Sync Processor conditions the input HS (horizontal synchronization) signal via a Schmitt buffer before output to the PLL and other functional blocks.

The interlaced mode recovery functions are disabled (power down) when not in use in order to provide for lower operating power.

NOTE: The MONO analog input pin is designed for an ac-coupled signal. The SVGA+ microdisplay does not provide the ac-coupling function, which is left to the display integrator. A dc-coupled input can be used provided the black level is maintained at a stable reference. Failure to do so will result in abrupt luminance changes and possible loss of synchronization.

Serial Interface

The serial interface consists of a serial controller and registers. The serial controller follows most of the I2C slave device protocol (clock stretching is not supported by this device). An internal address decoder transfers the content of the data into appropriate registers. The protocol will follow the address byte followed by register address data byte and register data byte sequence (3 bytes for each register access):

Serial address with write command

Register address

Register data

The registers are designed to be read/write. Read mode is accomplished via a 4 byte sequence:

Serial address with write command

Register address

Serial address with read command

Register data

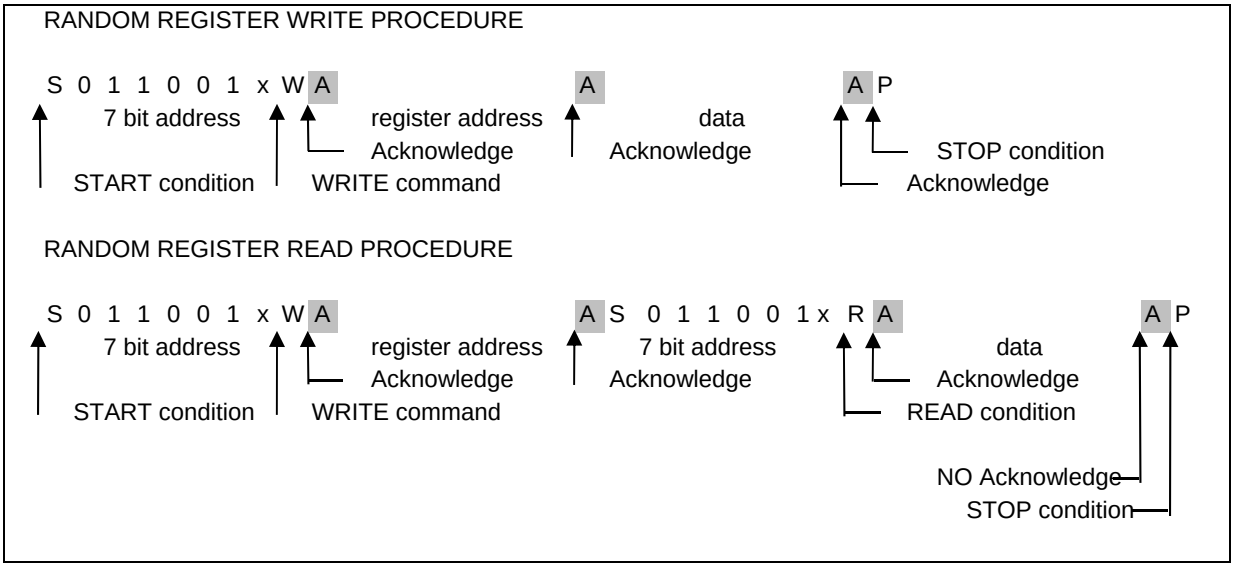


Figure 9-8. Serial Interface Protocol

The serial controller is capable of slave mode only.

The x in the 7-bit address code is set by the SERADD input pin and is provided to allow a dual display and single controller configuration. Slave Address: 011001X where X = 0 or 1 depending on the status of the SERADD pin.

Write Mode: Address is 64 (or 66 if SERADD = 1)

Read Mode: Address is 65 (or 67 is SERADD =1)

Sequential Read/Write Operation

The serial controller allows for both sequential and read operational modes. For either mode, the host needs only set the initial register address followed by as many data bytes as needed, taking care not to issue a STOP condition until all desired data bytes have been transmitted (or received).

Interface maximum frequency: 400 KHz.

Details of the timing of the SDA and SCL signals can be found in the I2C Standard, available on the Philips website.

The SDA pin is pulled up via a 2.2 Kilo-Ohm resistor that is mounted on the microdisplay carrier PCB.

Power On sequence

When VAN is applied without ramping to the OLED Microdisplay chip, the voltage at the gate of the current source is close to ground. As the storage capacitor is discharged to the reference level the current increases. Since the current source is on, current flows through the OLED and causes the flash seen when the display is initially turned on.

Ramping VAN to 3.3 volts before turning on VCOMMON allows the storage capacitor discharge to track the supply and keep the current source at or close to turn off. In addition, having VCOMMON at GND reduces the voltage that can be applied to the OLED to a maximum of VAN, and so this reduces the amount of current that can flow through the OLED.

To ensure proper startup and stabilization the following power-on sequence should be used:

1) Turn on VCC
2) Turn on VAN and wait for it to reach a minimum of 3.3V
3) Turn on VCOMMON

A 10 to 50 ms ramp is a good starting-point for implementation into a circuit design. Also, eMagin Corporation recommends that the registers are configured after VCC is up and before VAN and VCOMMON are brought up.

Power Down Modes

The circuit provides power down modes to minimize power consumption. Two modes of operations are provided to the user:-Automatic Power Down Mode

9.1.2. Automatic Power Down Mode

In the Automatic mode, functional blocks are powered down based on the display configuration. For example, in the power-up default mode, the sync separator and MONO input buffer blocks are automatically powered down.

9.1.3. Manual Power Down Mode

In the Manual mode, the user can, via the POWERDOWN and ATB registers, control independently the power down of most functional blocks. This mode is the preferred approach to set the microdisplay in its minimum power consumption mode, also known as sleep mode. To do so, the ATB7 bit must be set to VDD, and all bits of the POWERDOWN register must also be set to VDD. The contents of the registers will be preserved and the serial interface will remain functional.

9.1.4. VESA Modes

TABLE 9-5. VESA MODES

Mode		Frequency	Total	Active	Blanking	Front Porch + Border	Sync Pulse	Back Proch + Border
SVGA 800x600 85Hz non-interlaced	H	53.674KHz	1048 pixels	800 pixels	248 pixels	32 pixels	64 pixels	152 pixels
	V	85.061Hz	631 lines	600 lines	31 lines	1 line	3 lines	27 lines
	P	56.250MHz						
SVGA 800x600 75Hz non-interlaced	H	46.875KHz	1056 pixels	800 pixels	256 pixels	16 pixels	80 pixels	160 pixels
	V	75.000Hz	625 lines	600 lines	25 lines	1 line	3 lines	21 lines
	P	49.500MHz						
SVGA 800x600 72Hz non-interlaced	H	48.077KHz	1040 pixels	800 pixels	240 pixels	56 pixels	120 pixels	64 pixels
	V	72.188Hz	666 lines	600 lines	66 lines	37 lines	6 lines	23 lines
	P	50.000MHz						
SVGA 800x600 60Hz non-interlaced	H	37.879KHz	1056 pixels	800 pixels	256 pixels	40 pixels	128 pixels	88 pixels
	V	60.317Hz	628 lines	600 lines	28 lines	1 line	4 lines	23 lines
	P	40.000MHz						
VGA 640x480 85Hz non-interlaced	H	43.269KHz	832 pixels	640 pixels	192 pixels	56 pixels	56 pixels	80 pixels
	V	85.008Hz	509 lines	480 lines	29 lines	1 line	3 lines	25 lines
	P	36.000MHz						
VGA 640x480 75Hz non-interlaced	H	37.500KHz	840 pixels	640 pixels	200 pixels	16 pixels	64 pixels	120 pixels
	V	75.000Hz	500 lines	480 lines	20 lines	1 line	3 lines	16 lines
	P	31.500MHz						
VGA 640x480 72Hz non-interlaced	H	37.861KHz	832 pixels	640 pixels	192 pixels	24 pixels	40 pixels	128 pixels
	V	72.809Hz	520 lines	480 lines	40 lines	9 lines	3 lines	28 lines
	P	31.500MHz						
VGA 640x480 60Hz non-interlaced	H	31.469KHz	800 pixels	640 pixels	160 pixels	16 pixels	96 pixels	48 pixels
	V	59.940Hz	525 lines	480 lines	45 lines	10 lines	2 lines	33 lines
	P	25.175MHz						

Synchronization pulses (Hsync and Vsync) polarities must follow the VESA DMT standard.

TABLE 9-6. SYNCHRONIZATION PULSES POLARITY

Mode	VGA 60Hz	VGA 72Hz	VGA 75Hz	VGA 85Hz	SVGA 60Hz	SVGA 72Hz	SVGA 75Hz	SVGA 85Hz
Hsync Polarity	Negative	Negative	Negative	Negative	Positive	Positive	Positive	Positive
Vsync Polarity	Negative	Negative	Negative	Negative	Positive	Positive	Positive	Positive

9.1.5. Interlaced Video Modes

TABLE 9-7. INTERLACED VIDEO MODES

Mode		Frequency	Total	Active
170M 640 x480 30Hz interlaced	H	15.734 KHz	780 pixels	640 pixels
	V	30 Hz Frame / 60Hz Field	262.5 lines	240 lines
	P	12.27 MHz		
PAL 800x600 25 Hz interlaced	H	19.8 KHz	944 pixels	768 pixels
	V	25 Hz Frame / 50 Hz field	312.5 lines	288 lines
	P	14.75 MHz		

9.1.6. Zoom & 16:9 Modes

TABLE 9-8. ZOOM AND 16:9 VIDEO MODES

Mode		Frequency	Total	Active	Blanking	Front Porch	Sync Pulse	Back Porch
16:9 852x480 85Hz non-interlaced	H	43.265 KHz		852 pixels	192 pixels	56 pixels	56 pixels	80 pixels
	V	85.000Hz	509 lines	480 lines	29 lines	1 line	3 lines	25 lines
	P	45.168MHz						
16:9 852x480 75Hz non-interlaced	H	37.5 KHz	1052 pixels	852 pixels	200 pixels	16 pixels	64 pixels	120 pixels
	V	75.000Hz	500 lines	480 lines	20 lines	1 line	3 lines	16 lines
	P	39.45MHz						
16:9 852x480 60Hz non-interlaced	H	31.468KHz	1012 pixels	852 pixels	144 pixels	24 pixels	96 pixels	40 pixels
	V	59.94Hz	525 lines	480 lines	66 lines	16 lines	6 lines	23 lines
	P	31.84MHz						
Zoom 852x600 75Hz non-interlaced	H	46.875KHz	1108 pixels	852 pixels	256 pixels	16 pixels	80 pixels	160 pixels
	V	75.0Hz	625 lines	600 lines	25 lines	1 line	3 lines	21 lines
	P	51.937MHz						
Zoom 852x600 60Hz non-interlaced	H	37.642KHz	1108 pixels	852 pixels	256 pixels	40 pixels	128 pixels	88 pixels
	V	59.94Hz	628 lines	600 lines	28 lines	1 line	4 lines	23 lines
	P	41.707MHz						

Synchronization pulses polarities for Zoom and 16:9 modes

TABLE 9-9. ZOOM AND 16:9 MODES SYNCHRONIZATION PULSES POLARITY

Mode	Zoom 60Hz	Zoom 75Hz	16:9 60Hz	16:9 75Hz	16:9 85Hz
Hsync Polarity	Negative	Negative	Negative	Negative	Negative
Vsync Polarity	Negative	Negative	Negative	Negative	Negative

10. REGISTER MAP SUMMARY

Register Index (Hex)	Name	Access	Bit Name	Bit#	Reset Value (Hex)	Description
00	STAT	R	LOCK	7	-	PLL Lock Flag, 1=Locked, 0=Not Locked
			STAT[6:3]	6-3	0	Reserved
			REV	2-0	1	Silicon Revision Number
01	RGAIN	R/W	RGAIN	7-0	80	+/- 50% Red channel gain control
02	ROFF	R/W	ROFF7	7	0	Reserved
			ROFF	6-0	40	+/- 50% Red channel offset control
03	GGAIN	R/W	GGAIN	7-0	80	+/- 50% Green channel gain control
04	GOFF	R/W	GOFF7	7	0	Reserved
			GOFF	6-0	40	+/- 50% Green channel offset control
05	BGAIN	R/W	BGAIN	7-0	80	+/- 50% Blue channel gain control
06	BOFF	R/W	GOFF7	7	0	Reserved
			BOFF	6-0	40	+/- 50% Blue channel offset control
07	MGAIN	R/W	MGAIN	7-0	80	+/- 50% Mono channel gain control
08	MOFF	R/W	MOFF7	7	0	Reserved
			MOFF	6-0	40	+/- 50% Mono channel offset control
09	VMODE	R/W	SRESET	7	0	Software Reset. Clears all registers to default setting, powerdowns analog blocks and holds until released (1)
			VSCANS	6	0	Vertical Scan Direction Source. 1=VMODE5, 0=U/D
			VSCAN	5	0	Vertical Scan Direction. 1=Up, 0=Down
			VSEL	2-4	0	Vertical Sequence Mode select
			COLSEL	1-0	0	Color Mode. 00=rgb, 01=white, 10=composite
0A	HMODE	R/W	HSOFT	7	1	Burn-in Compensation Enable
			HMODE6	6	0	Reserved
			CLKS	5	0	Clock Source. 1=VCLK, 0=PLL
			HSCANS	4	0	Horizontal Scan Direction Source. 1=HMODE3, 0=L/R
			HSCAN	3	0	Horizontal Scan Direction. 0=Left, 1=Right
			HSEL	2-0	4	Horizontal Mode Select.
0B	BR_L	R/W	BR[7:0]	7	0	Reserved
0C	BR_U	R/W	BR[15:8]	7	80	Reserved
0D	HRATE_L	R/W	HRATE[7:0]	7-0	0	Horizontal Frame Shift Rate Counter lower bits
0E	HRATE_U	R/W	HRATE[15:8]	7-0	80	Horizontal Frame Shift Rate Counter upper bits
0F	PLL_L	R/W	FBD[7:0]	7-0	52	PLL Feedback Divider lower bits
						(Continued)
10	PLL_U	R/W	ICPSEL[1:0]	7-6	1	Charge Pump Current Control

			PLL_U5	5	0	Reserved
			PSD[1:0]	4-3	1	PLL Post Scaler Divider Register
			FBD[10:8]	2-0	4	PLL Feedback Divider upper bits
11	PIF	R/W	BREFQ[4:0]	7-4	8	Luminance control base frequency register
			PIF[3:0]	3-0	1	Pixel Clock Frequency Selection. Default is Zoom 60 Hz (41.707 MHz)
12	PI2	R/W	PIBYP	7	0	Phase Interpolator Bypass. 1=Bypassed, 0= Not bypassed
			PHSEL[1:0]	6-5	0	PLL Clock phase selection when PIBYP = 1 (90° phase selection)
			PHASE[4:0]	4-0	0	PLL Clock phase adjustment when PiBYP =0 (32 steps)
13	HSTART	R/W	HSTART[7:0]	7-0	D3	Horizontal Active Start Counter
14	VSTART	R/W	VSTART5:0]	5-0	18	Vertical Active Start Counter
			VSTART[7:6]	7-6	0	Reserved
15	HBLK	R/W	HBLK[7:0]	7-0	80	Reserved.
16	HDEL	R/W	HDEL[7:0]	7-0	0C	Reserved.
17	PDWN	R/W	PDWN7	7	0	Bias block power down. 1=Power Down
			PDWN6	6	0	VBLACK Buffer power down. 1=Power Down
			PDWN5	5	0	VBH Buffer power down. 1=Power Down
			PDWN4	4	0	VBL Buffer power down. 1=Power Down
			PDWN3	3	0	Phase Interpolator Power down. 1=Power Down
			PDWN2	2	0	PLL Power downs. 1=Power Down
			PDWN1	1	1	Mono Channel power down. 1=Power Down
			PDWN0	0	0	RGB Channels power down. 1=Power Down
18	ATB	R/W	ATB7	7	0	Power Down Source. 1=PWDN Register, 0=Internal
			ATB[6..0]	6-0	0	Reserved.
19	AMTEST	R/W	AMTEST[7:0]	7-0	0	Reserved.
1A	TRIM	R/W	TRIM[7:0]	7-0	60	Reserved.

Figure 10-1. Register Map Summary

Note: Reserved registers have a default power-on value and do not need to be updated. These registers are meant for device test and should be left as is. Attempts at writing any of these registers may lead to permanent functional damage to the microdisplay.

11. DETAILED REGISTER DESCRIPTION

Name: **STATUS**
Index: **0h**
Mode: **Read Only**

Bit Name	Bit#	Reset Value	Description
REV	0-2	01h	Circuit Revision. Initial Value is 000. Will increase by +1 for each all-layer change.
STAT [6:3]	3-6	00h	Reserved
LOCK	7	N/A	PLL lock status

Bit	Name	Description
7	LOCK	PLL Lock Status 0 = Unlocked 1 = Locked

Name: **RGAIN**
Index: **01h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
RGAIN	0-7	80h	Red Data Channel gain control

Bit	Name	Description
0-7	RGAIN	Controls the gain of the Red Analog Input. The 8-bit value spans a range of one half to one and a half the signal's full-scale value. The default (reset) value is a gain of 1 (80h value).

Name: **ROFF**
Index: **02h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
ROFF	0-6	40h	Red Data Channel offset control

Bit	Name	Description
0-6	ROFF	Controls the dc offset of the Red Analog Input. The 6-bit value spans a range of one half to one and a half the signal's full-scale value. The default (reset) value is zero offset (40h value).
7	ROFF7	Reserved

Name: **GGAIN**
Index: **03h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
GGAIN	0-7	80h	Green Data Channel gain control

Bit	Name	Description
0-7	GGAIN	Controls the gain of the Green Analog Input. The 8-bit value spans a range of one half to one and a half the signal's full scale value. The default (reset) value is a gain of 1 (80h value).

Name: **GOFF**
Index: **04h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
GOFF	0-6	40h	Green Data Channel offset control

Bit	Name	Description
0-6	GOFF	Controls the dc offset of the Green Analog Input. The 6-bit value spans a range of one half to one and a half the signal's full-scale value. The default (reset) value is zero offset (40h value).
7	GOFF7	Reserved

Name: **BGAIN**
Index: **05h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
BGAIN	0-7	80h	Blue Data Channel gain control

Bit	Name	Description
0-7	BGAIN	Controls the gain of the Blue Analog Input. The 8-bit value spans a range of one half to one and a half the signal's full scale value. The default (reset) value is a gain of 1 (80h value).

Name: **BOFF**
Index: **06h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
BOFF	0-6	40h	Blue Data Channel offset control

Bit	Name	Description
0-6	BOFF	Controls the dc offset of the Blue Analog Input. The 6-bit value spans a range of one half to one and a half the signal's full-scale value. The default (reset) value is zero offset (40h value).
7	BOFF7	Reserved

Name: **MGAIN**
Index: **07h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
MGAIN	0-7	80h	Mono Data Channel gain control

Bit	Name	Description
0-7	MGAIN	Controls the gain of the Mono Analog Input. The 8-bit value spans a range of one half to one and a half the signal's full scale value. The default (reset) value is a gain of 1 (80h value).

Name: **MOFF**
Index: **08h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
MOFF	0-6	40h	Mono Data Channel offset control

Bit	Name	Description
0-6	MOFF	Controls the dc offset of the Mono Analog Input. The 6-bit value spans a range of one half to one and a half the signal's full-scale value. The default (reset) value is zero offset (40h value).
7	MOFF7	Reserved

Name: **VMODE**
Index: **09h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
COLSEL	0-1	00h	Color Mode Selection
VSEL	2-4	00h	Vertical Sequence Mode Selection
VSCAN 5	0		Vertical Scan Direction Selection
VSCANS	6	0	Vertical Scan Direction Source Selection
SRESET	7	0	Software Reset, active high bit

Bit	Name	Description
0-1	COLSEL	Determine which data input is used (RGB or MONO) and the chromaticity of the RGB mode (color or white only).

COLSEL 1	COLSEL 0	Color Mode
0	0	R,G,B inputs selected (Default)
0	1	White-Only Mode selected
1	0	MONO input selected
1	1	R,G,B inputs selected

The White-only mode selection will result in every subpixel of a color group to be addressed with the normalized sum of the R, G, and B input signals. This mode should be selected only for monochrome white applications or for microdisplay specially ordered without color filters.

Bit	Name	Description
2-4	VSEL	Determine the Vertical Mode for the display operation. Default is SVGA.

VSEL2	VSEL1	VSEL 0	Vertical Mode
0	0	0	SVGA / Zoom (600 Rows)
0	0	1	VGA / 16:9 (480 Rows)
0	1	0	Interlaced 2 (600 Rows)
0	1	1	Pseudo Interlaced 2 (600 Rows)
1	0	0	Interlaced 1 (480 Rows)
1	0	1	Pseudo Interlaced 1 (480 Rows)
1	1	0	SVGA / Zoom (600 Rows)
1	1	1	SVGA / Zoom (600 Rows)

5 VSCAN Determines the vertical scan direction. Default is Scan Down (0).
0 = Scan Down: Top to Bottom
1 = Scan Up: Bottom to Top

6 VSCANS Determines the source of the vertical direction control: Bit5 or the U/D external pin. Default is the U/D external pin.
1 = Direction determined by status of VSCAN
0 = Direction determined by status of U/D pin
GND = Scan Down: top to bottom
VDD = Scan Up: bottom to top

7	SRESET	Circuit software reset. When active, resets all the circuit's registers and power downs all functional blocks except the serial interface. The circuit will remain in this reset state until SRESET is deactivated. When coming out of reset, the circuit will self-initialize to the SVGA, 60Hz mode. Default value is deactivated. 0 = SRESET inactive 1 = SRESET active

Name: **HMODE**
Index: **0Ah**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
HSEL	0-2	04h	Horizontal Mode Selection
HSCAN	3	0	Horizontal Scan Direction Selection
HSCANS	4	0	Horizontal Scan Direction Source Selection
CLKS	5	0	Circuit System Clock Source Selection
HMODE6	6	0	Reserved
HSOFT	7	1	Screen Saver Enable

Bit	Name	Description
0-2	HSEL	Determines the horizontal mode for the display. Default is SVGA.

HSEL2	HSEL1	HSEL 0	Horizontal Mode
0	0	0	Interlaced 2 /Pseudo Interlaced 2 (800 Columns)
0	0	1	VGA / Interlaced 1 / Pseudo Interlaced 1 (640 Columns)
0	1	0	SVGA (800 Columns)
0	1	1	Interlaced 2 /Pseudo Interlaced 2 (800 Columns)
1	X	X	16:9 & zoom (852Columns)

.

3	HSCAN	Determines the horizontal scan direction. Default is Scan Right (0). 0 = Scan Right: Left to Right 1 = Scan Left: Right to Left
4	HSCANS	Determines the source of the horizontal direction control: Bit3 or the U/D external pin. Default is U/D external pin. 1 = Direction determined by status of HSCAN 0 = Direction determined by status of L/R pin GND = Scan Right: left to right VDD = Scan Left: right to left
5	CLKS	Determines the source of the circuit system clock: PLL or the VCLK external pin. Default is internal (PLL) 0 = Clock source is internal PLL 1 = Clock source is external pin VLCK When CLKS = 1, the PLL and Phase Interpolator are powered-down.

Bit	Name	Description
6	HMODE6	Reserved
7	HSOFT	Activates /deactivates the horizontal screen saver mode. When activated, the image frame will be moved left to right and right to left over a 5 pixel span at a rate determined by the value of HRATE (See below, register index 0Eh and 0Fh). This mode is not applicable to the horizontal Zoom mode. Default is screen saver mode activated. 0 = Screen saver mode deactivated 1 = Screen saver mode activated

Name: **BR_L / BR_U**
Index: **0Bh, 0Ch**
Mode: **Read-Write**

Bit Name	Index	Bit#	Reset Value	Description
BR_L [7:0]	0Bh	0-7	00h	Reserved
BR_U [7:0]	0Ch	0-7	02h	Reserved

These registers are reserved for wafer level testing and are of no use for normal operation.

Name: **HRATE_L / HRATE_U**
Index: **0Dh, 0Eh**
Mode: **Read-Write**

Bit Name	Index	Bit#	Reset Value	Description
HRATE [7:0]	0Dh	0-7	00h	Horizontal Frame Shift Rate LSBs
HRATE [15:8]	0Eh	0-7	80h	Horizontal Frame Shift Rate MSBs

The value that is programmed into HRATE [15:0] determines, in units of vertical periods, the rate of single column shift (left or right) for the display frame. An internal 16-bit counter advances at every Vsync until its output equals the value programmed into HRATE [15:0]. At that time, the display frame is shifted by one column. The Default value is 8000h, which for a 60Hz refresh rate corresponds to one shift every 546 seconds or approximately 9 minutes.

Name: **PLL_L / PLL_U**
Index: **0Fh, 10h**
Mode: **Read-Write**

Bit Name	Index	Bit#	Reset Value	Description
FBD [7:0]	0Fh	0-7	52h	PLL Feedback Divider LSBs
FBD [10:8]	10h	0-2	04h	PLL Feedback Divider MSBs
PSD [1:0]	10h	3-4	01h	PLL Post-Scaler Divider
PLL_U [7:5]	10h	5-7	00h	Reserved

The value that is programmed into FBD [10:0] is equal to the number of pixel clock period per horizontal period minus 2. For instance if a total of 1056 clock periods per line is desired (this number is the default SVGA 60Hz mode), then the value programmed into FBD [10:0] is 1054 or 41Eh. Small adjustments with count may be necessary to compensate for variations between different implementations of the standards.

The value that is programmed into PSD [1:0] is the divider factor for the VCO clock output before it is routed to the Phase Interpolator module.

PSD1	PSD0	PSD Divider
0	0	2
0	1	4
1	0	8
1	1	16

The default value after reset is PSD[1:0] = 01 (divide by 4).

Note: The internal oscillator has a maximum internal frequency of 200 MHz. Any combination of FBD [10:0] and PSD [1:0] that would result in the oscillator exceeding that frequency should be avoided to prevent permanent damage to the circuit.

Name: **PIF**
Index: **11h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
PIF [3:0]	0-3	0Ch	Phase Interpolator Reference Frequency Selection
PIF [7:4]	4-7	00h	Reserved

Bit	Name	Description
0-3	PIF [3:0]	Determines the reference pixel clock frequency for the phase interpolator Default value is SVGA 60Hz (40 MHz)

PIF3	PIF2	PIF1	PIF0	Pixel Clock Frequency & Mode
0	0	0	0	Reserved
0	0	0	1	41.707 MHz – Zoom 852x600 @60Hz
0	0	1	0	51.937 MHz – Zoom 852x600 @75Hz
0	0	1	1	31.84 MHz – 852x480 @60Hz
0	1	0	0	39.45 MHz – 852x480 @75Hz
0	1	0	1	45.168 MHz – 852x480 @85Hz
0	1	1	0	14.75 MHz – PAL @25Hz
0	1	1	1	12.275 MHz – SMPTE170M @30Hz
1	0	0	0	25.175 MHz – VGA 640x480 @60Hz
1	0	0	1	31.50 MHz – VGA 640x480 @72Hz
1	0	1	0	31.50 MHz – VGA 640x480 @75Hz
1	0	1	1	36.0 MHz – VGA 640x480 @85Hz
1	1	0	0	40.0 MHz – SVGA 800x600 @60Hz
1	1	0	1	50.0 MHz – SVGA 800x600 @72Hz
1	1	1	0	49.5 MHz – SVGA 800x600 @75Hz
1	1	1	1	56.25 MHz – SVGA 800x600 @85Hz

Note: When setting the FBD and PSD values, the user must select the matching PIF setting. For modes other than those directly supported by the SVGA+ Microdisplay (and mentioned above), there is no guarantee of performance even if the PIF setting is set to the closest value of the programmed frequency output.

4-7	PIF [7:4]	Reserved

Name: **PI2**

Index: **12h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
PHASE	0-4	00h	PLL Clock Phase Adjustment when PIBYP = 0
PHSEL	5-6	00h	PLL Clock Phase Adjustment when PIBYP = 1
PIBYP	7	0	Phase Interpolator bypass selection.

Bit	Name	Description
0-4	PHASE	Selects the clock edge offset in 32 discrete steps from zero to one clock period. This selection is active only when PIBYP = 0.
5-6	PHSEL	Selects one of 4 clock edge offsets when PIBYP = 1.

PHSEL1	PHSEL 0	Clock Edge Offset
0	0	None
0	1	90°
1	0	180°
1	1	270°

7	PIBYP	Phase Interpolator Bypass Enable. When active (High) the Phase interpolator circuit is bypassed and only 4 phase shifts are available. The PIBYP mode can be used when a simple adjustment is sufficient, allowing the PI circuit to be powered down.

Name: **HSTART**
Index: **13h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
HSTART	0-7	D3h	Horizontal Active Start Count

The value that is programmed into HSTART sets the number of clock cycles after the leading edge of Hsync at which the analog input signal will be sampled into the Microdisplay, minus 5. This gap is equivalent to the sum of the Sync pulse width plus the Back Porch (as defined in the VESA Display Monitor Timing Specification).

Name: **VSTART**
Index: **14h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
VSTART	0-5	18h	Vertical Active Start Count
VSTRT[7:6]	6-7	00h	Reserved

The value that is programmed into VSTART sets the number Hsync after the leading edge of Vsync at which the first analog input signal line will be sampled into the Microdisplay, minus 3. This gap is equivalent to the sum of the Sync pulse width plus the Back Porch (as defined in the VESA Display Monitor Timing Specification).

Name: **HBLK**
Index: **15h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
HBLK [7:0]	0-7	80h	Reset to black pulse width

The value that is programmed into HBLK sets the width in Tclk increments of a "reset to black" duration at the beginning of each display row. The higher the value, the longer the reset duration. This setting minimizes residual charge in the array matrix that could contribute to ghost images or crosstalk. The default value has been calculated for the SVGA 60Hz format.

Name: **HDEL**
Index: **16h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
HDEL [7:0]	0-7	0Ch	Break before make switch delay

The value that is programmed into HDEL sets the gap between the closure of two of the analog switches used in the pixel driver. The default value should not be changed for normal operation.

Name: **POWERDOWN**
Index: **17h**
Mode: **Read-Write**

Bit Name	Bit#	Reset Value	Description
PWRDN0	0	0	RGB Channels power down enable
PWRDN1	1	1	MONO Channel power down enable
PWRDN2	2	0	PLL power down enable
PWRDN3	3	0	Phase Interpolator power down enable
PWRDN4	4	0	VBL Buffer power down enable
PWRDN5	5	0	VBH Buffer power down enable
PWRDN6	6	0	VBLACK Buffer power down enable
PWRDN7	7	0	Bias block power down enable

Bit	Name	Description

0	PWRDN0	Active only when ATB7 = 1. When active (high), disables and powers down the R, G, and B analog input channels. No input at the RED, GREEN and BLUE pins will be processed while PWRDN0 = 1. When ATB7 = 0, PWRDN0 has not effect. The R, G, B channels will be powered down if the MONO channel is selected via VSEL [1:0] Default after reset is PWRDN0 = 0.
1	PWRDN1	Active only when ATB7 = 1. When active (high), disables and powers down the MONO analog input channel. No input at the MONO input pin will be processed while PWRDN1 = 1. The sync separator circuit will also be disabled. When ATB7 = 0, PWRDN1 has not effect. The MONO channel will be powered down if the R,G,B channels are selected via VSEL[1:0] Default after reset is PWRDN1 = 1.
2	PWRDN2	Active only when ATB7 = 1. When active (high), disables and powers down the internal PLL circuit. No clock will be recovered from Hsync while PWRDN2 = 1. When ATB7 = 0, PWRDN2 has no effect. The PLL will be powered down if the VCLK pin is selected as the clock source (CLKS = 1). Default after reset is PWRDN2 = 0.
3	PWRDN3	Active only when ATB7 = 1. When active (high), disables and powers down the Phase Interpolator circuit. No fine adjustment of the clock phase can be effected while PWRDN3 = 1. Only the simple adjustments controlled by PHSEL[1:0] can be used. When ATB7 = 0, PWRDN3 has not effect. The Phase Interpolator will be powered down if the PIBYP bit is set. Default after reset is PWRDN0 = 0.
4	PWRDN4	Active only when ATB7 = 1. When active (high), disables and powers down the VBL Output Buffer. The VBL pin can then used as an input pin while PWRDN4 = 1. When ATB7 = 0, PWRDN4 has not effect on the VBL buffer. Default after reset is PWRDN4 = 0.
5	PWRDN5	Active only when ATB7 = 1. When active (high), disables and powers down the VBH Output Buffer. The VBH pin can then used as an input pin while PWRDN5 = 1. When ATB7 = 0, PWRDN5 has not effect on the VBH buffer Default after reset is PWRDN2 = 0.
6	PWRDN6	Active only when ATB7 = 1. When active (high), disables and powers down the VBLACK Output Buffer. The VBLACK pin can then used as an input pin while PWRDN6 = 1. When ATB7 = 0, PWRDN6 has not effect on the VBLACK buffer. Default after reset is PWRDN6 = 0.
7	PWRDN7	Active only when ATB7 = 1. When active (high), disables and powers down the Bias circuit. While PWRDN7 = 1 no internal bias levels or current will be generated, preventing all circuit operation except for the digital only blocks such as the serial interface and register controller. When ATB7 = 0, PWRDN7 has no effect. Default after reset is PWRDN7 = 0.

Name: ATB
Index: 18h
Mode: Read-Write

Bit Name	Bit#	Reset Value	Description
ATB [6,4:0]	0-4,6	00h	Reserved for internal use
ATB5	5	0	MONO Input Bias Source Selection
ATB7	7	0	Power down source selection: External /Automatic

Bit	Name	Description
0-6	ATB [6,4:0]	Reserved
5	ATB5	Active high input used to set the black level bias when selecting the MONO input channel. ATB5 must be set to 1 (logic high level) in order to properly set the black level reference for this mode. ATB5 must be set to 0 (logic low level) for modes using the R, G, B inputs.
7	ATB7	Active high enable for using the POWERDOWN register as the controlling source for circuit block power downs. When ATB7 = 0, functional blocks are powered down based on the VMODE and HMODE register settings. When ATB7 = 1, the settings in the POWERDOWN register control the functional blocks power down state. Default after reset is PWRDN0 = 0.

Name: AMTEST
Index: 19h
Mode: Read-Write

Bit Name	Bit#	Reset Value	Description
AMTEST	0-7	00h	Reserved for testing

This register is reserved for wafer level testing and is of no use for normal operation.

Bit	Name	Description
7	AMTEST[7:0]	Reserved

Name: TRIM
Index: 1Ah
Mode: Read-Write

Bit Name	Bit#	Reset Value	Description
TRIM [7:5]	5-7	03h	Trim value read back (read only)
TRIM [4]	4	0	Trim mode: continuous / startup
TRIM [3]	3	0	Trim override enable (active high)
TRIM [2:0]	0-2	00h	Trim override input

The TRIM register controls an internal calibration resistor used by the Input Buffer circuit and aimed at compensating non-linearities in the silicon.
The default configuration is for an automatic and periodic calibration (every Vsync). An override bit allows the user to modify the trim resistor setting with the 3 least significant bits.

12. REGISTER TABLE CONFIGURATION

Recommended values for use with on-chip PLL selected.
For use with external clock, change bit 5 of HMODE from 0 to 1.

VESA Modes

TABLE 12-1. VESA MODES REGISTER SETTINGS

NAME	ADDRESS	SVGA_60	SVGA_72	SVGA_75	SVGA_85	VGA_60	VGA_72	VGA_75	VGA_85
STATUS	00	00	00	00	00	00	00	00	00
RGAIN	01	78	78	78	78	78	78	78	78
ROFF	02	30	30	30	30	30	30	30	30
GGAIN	03	78	78	78	78	78	78	78	78
GOFF	04	30	30	30	30	30	30	30	30
BGAIN	05	78	78	78	78	78	78	78	78
BOFF	06	30	30	30	30	30	30	30	30
MGAIN	07	80	80	80	80	80	80	80	80
MOFF	08	38	38	38	38	38	38	38	38
VMODE	09	00	00	00	00	04	04	04	04
HMODE	0A	02	02	02	02	01	01	01	01
BR_L	0B	00	00	00	00	00	00	00	00
BR_U	0C	02	02	02	02	02	02	02	02
HRATE_L	0D	00	00	00	00	00	00	00	00
HRATE_U	0E	80	80	80	80	80	80	80	80
PLL_L	0F	1E	0E	1E	16	1D	3E	46	3E
PLL_U	10	0C	04	0C	04	0B	0B	0B	0B
PIF	11	0C	0D	0E	0F	08	09	0A	0B
PI2	12	00	00	18	18	18	18	18	18
HSTART	13	D4	B4	EC	D4	8B	A4	B4	84
VSTART	14	19	DB	16	1C	21	1D	11	1A
HBLK	15	D8	D8	D8	D8	D8	D8	D8	D8
HDEL	16	0C	0C	0C	0C	0C	0C	0C	0C
PWDN	17	02	02	02	02	02	02	02	02
ATB	18	80	80	80	80	80	80	80	80
AMTEST	19	00	00	00	00	00	00	00	00
TRIM	1A	08	08	08	08	08	08	08	08

Note: The last two digits after the video format indicate the refresh rate in Hz.

TABLE 12-2. NON-VESA MODES REGISTER SETTINGS

NAME	ADDRESS	ZOOM_60	ZOOM_75	DVD_60	DVD_75	DVD_85	NTSC/170	PAL
STATUS	00	00	00	00	00	00	00	00
RGAIN	01	78	78	78	78	78	78	78
ROFF	02	30	30	30	30	30	30	38
GGAIN	03	78	78	78	78	78	78	78
GOFF	04	30	30	30	30	30	30	38
BGAIN	05	78	78	78	78	78	78	78
BOFF	06	30	30	30	30	30	30	38
MGAIN	07	80	80	80	80	80	80	81
MOFF	08	38	38	38	38	38	38	39
VMODE	09	00	00	04	04	04	12	4A
HMODE	0A	04	04	04	04	04	01	10
BR_L	0B	00	00	00	00	00	00	00
BR_U	0C	02	02	02	02	02	80	02
HRATE_L	0D	00	00	00	00	00	00	00
HRATE_U	0E	80	80	80	80	80	80	80
PLL_L	0F	51	52	F1	1A	12	0A	AE
PLL_U	10	0C	0C	0B	0C	0C	1B	13
PIF	11	01	02	03	04	05	07	07
PI2	12	00	12	04	18	14	08	00
HSTART	13	D3	EC	83	B4	84	7B	90
VSTART	14	19	16	1B	11	1A	0F	0F
HBLK	15	D8	D8	D8	D8	D8	D8	D8
HDEL	16	0C	0C	0C	0C	0C	0C	0C
PWDN	17	02	02	02	02	02	01	71
ATB	18	80	80	80	80	80	20	80
AMTEST	19	00	00	00	00	00	00	00
TRIM	1A	08	08	08	08	08	08	08

Notes:

1. The last two digits after the video format indicate the refresh rate in Hz.
2. Zoom stands for an 852 x 600 format
3. DVD stands for an 852 x 480 format
4. PAL settings support the following PAL standards: I, B, G, H, D, N. Use NTSC settings for PAL M.

13. APPENDIX A: MICRODISPLAY CARRIER BOARD ELECTRICAL DIAGRAM

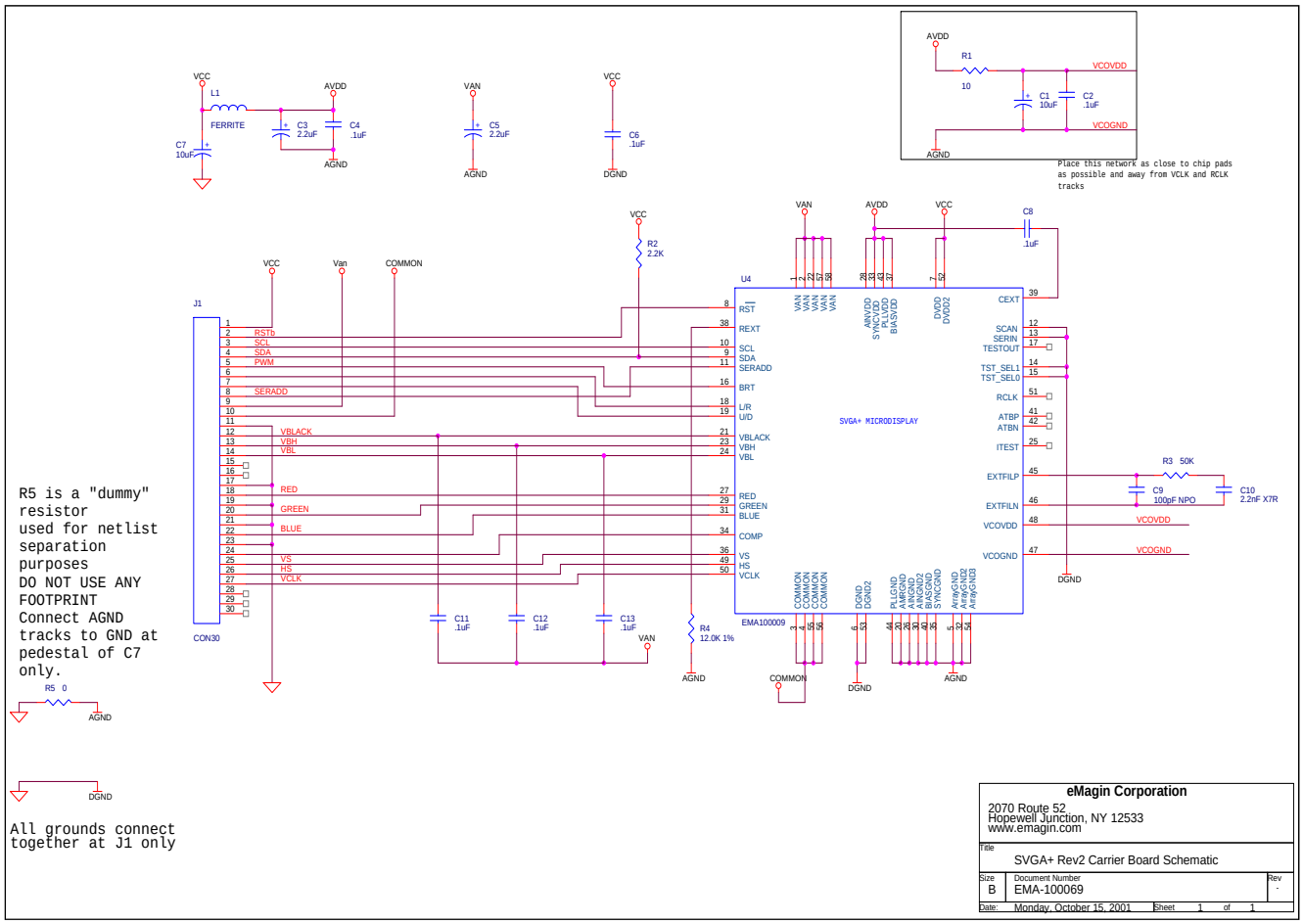


Figure 13-1. Microdisplay Carrier Board Electrical Diagram

14. APPENDIX B: COMPOSITE SIGNAL INPUT CONNECTIONS

TABLE B-1. MINIMUM CONNECTIONS REQUIRED FOR COMPOSITE INPUT

Pin	Notes
Pin 1	Power
Pin 2	Reset should be pulled high through an RC network to VDD to ensure that reset stays on low for 100 µsecs after all other lines have stabilized.
Pin 3	2.2kΩ pull-up to VDD
Pin 4	(Note: there is a 2.2kΩ pull-up resistor on the display board)
Pin 6	Should be grounded for normal operation
Pin 7	Should be grounded for normal operation
Pin 8	Should be grounded for normal operation
Pin 9	Power
Pin 10	Power
Pin 11	Ground
Pin 17	Ground
Pin 19	Ground
Pin 21	Ground
Pin 23	Ground
Pin 24	For mono NTSC input attach a .01µF ceramic coupling capacitor. A 75Ω termination resistor to ground on the signal side of the capacitor is recommended to prevent reflection and noise in the transmission line.

After the chip has reset (enters the high state), load the NTSC settings into the registers through the I^2C serial bus. Anytime the chip is reset, the register values must be reloaded.

15. APPENDIX C: REVISION HISTORY

Revision Level	Date	Scope
-	04-20-01	Initial Release
1	05-10-01	Register Table Update, Syncs Polarity definition
2	09-19-01	Silicon Version 2 Update, All pages, New P/N
3	09-09-03	Clarifications and correction of typographical errors
4	01-09-04	Updated VESA Mode Register Settings/Configurations
5	01-29-04	Updated non-VESA Mode Register Settings
6	04-15-04	General update of most sections; Replaced Mechanical Drawing with Revision C
7	06-21-04	Replaced Mechanical Drawing with Revision E
8	06-25-04	Edits to Electrical Characteristics Section
9	11-29-05	• Expanded CIE specification of the SVGA+ color microdisplay to standardize this parameter for all color microdisplays in the SVGA Series (Tables 2-1, 6-1) • Added measurement conditions for luminance, contrast and chromaticity (Page 10) • Provided additional detailed information regarding pixel driver operation (Page 17) • Provided detailed information regarding internal and external voltage references (Pages 17-20; Tables 5-1, 5-2, 5-3; Figure 3-1) • Replaced MONO_600 mode with register settings for PAL signals (Page 36; Tables 3-1, 9-7, 12-2) • Added recommended power-on sequence (previously provided as Application Note) to avoid flash (Page 25) • Reset value corrections for the following registers: STAT [2-0], PLL_L [7-0], HSTART [7-0], VSTART [5-0], HBLK [7-0], TRIM [7-0] (Pages 30, 35, 37-38, 40; Figure 10-1) • Necessary connections for composite signals added as Appendix B
10	11-25-09	• Made corrections to timing and frame rate for the PAL standard (Tables 9-7, 12-2) • Changed recommended TRIM register settings from 00h to 08h for all modes. This disables an automatic trim resistor compensation routine for more consistent contrast across microdisplays. • Replaced External Reference Circuit Diagram with version showing Vcc voltage (Figure 9-5) • Removed CIE specification from Table 2-1. Values are located in Tables 6-1 through 6-4. • Changed document formatting for easier navigation through text. • Removed separate electrical levels for Hs, Vs Table 5.3 • Make reference to the Defect Criteria document and added cleaning, handling and storage recommendations in section 8.0
11	4/29/10	• Updated Microdisplay Assembly Drawing on Page 13 to reflect current Die and Adhesive tolerance
12	8/18/10	• Updated Figure 7.1 Assembly Drawing for consistency with all SVGA+ Datasheets
13	2/10/16	• Updated Table 5.2 for minimum Van level

		• Removed Yellow and Green from product specification (obsolete)