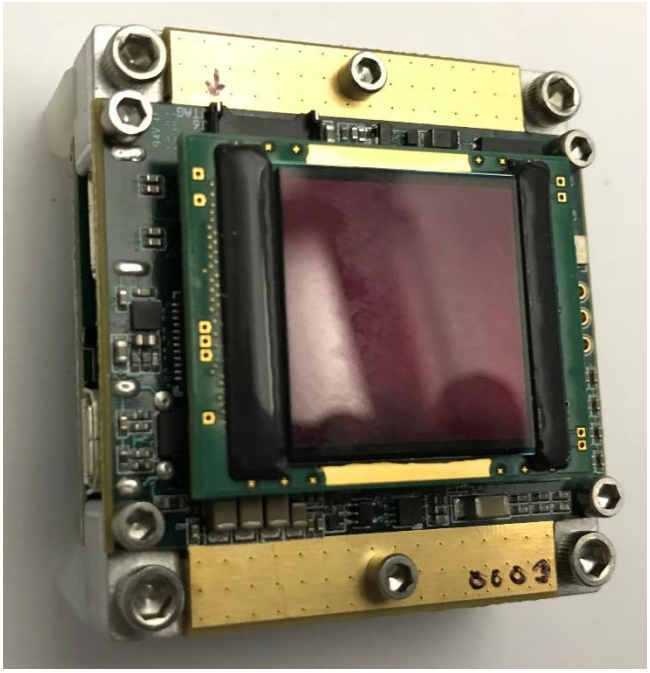
2K X 2K COMPACT INTERFACE



DATASHEET
Rev A

For Part Numbers:

EMA-101304-01
EMA-101306-01
EMA-101307-01

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Revision Level	ECN	Date	Scope
1		June 2018	Draft Release
-	000815	September 2019	Initial Release
A	000988	July 2020	Corrected serial interface speed p. 15

TABLE OF CONTENTS

1. SCOPE

This document describes the electrical, mechanical and programmatic characteristics of the 2K x 2K Compact Interface assembly.

2. GENERAL DESCRIPTION

The 2K x 2K Compact Interface (2K_CI), part number EMA-200024, provides the user with a compact and portable means of operating an eMagin 2K x 2K OLED Microdisplay, using a DisplayPort 1.2a compliant data interface. The included resident firmware provides access to the microdisplay's on-board register settings from any Windows-based PC through a USB port and supports all different types of 2K x 2K OLED Microdisplays. A single 9V DC power input is required to operate the 2K x 2K Compact Interface

3. MAIN FEATURES

3.1 Hardware Features

- Compact form factor 43 x 46 x 18 mm
- Two-board stack configuration
- DisplayPort 1.2a compatible input video data
- USB 2.0 interface allows access to interface and microdisplay registers
- Mounting holes at corners to facilitate system integration
- Built-in heat spreader can be used to connect external heatsink as needed

3.2 Software Features

- Automatic format configuration at power-on
- Automatic valid input data detection
- Read/write capabilities allow adjustments of interface register settings to fine-tune image characteristics
- Brightness and custom gamma adjustments
- Save feature stores custom register settings for convenience

4. FUNCTIONAL OVERVIEW

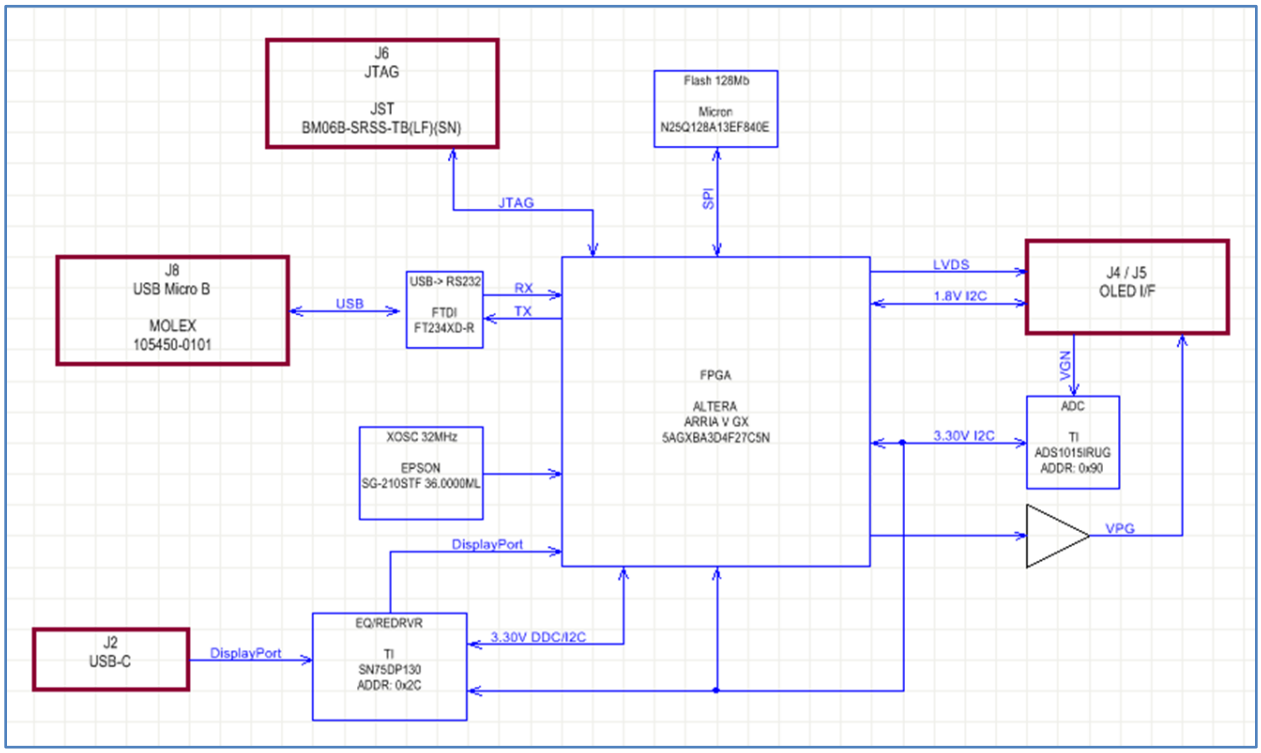

Figure 1: Top-level FPGA Board Block Diagram

The 2K x 2K Compact Interface (2K_CI) is made of two circuit board assemblies:

- Power board assembly that converts the input DC power into the various supply levels required by both the 2K-CI and the 2K x 2K Microdisplay

- FPGA board assembly that processes the incoming DisplayPort data and USB controls to configure and control the 2K x 2K Microdisplay

4.1 Power Board Assembly

The power board assembly generates nine supply rails ranging from -1.5VDC to +5VDC
The voltage conversion is handled by switching regulators followed by low dropout regulators to ensure minimum voltage ripple during operation.

4.2 FPGA Board Assembly

The FPGA board assembly is designed around an Altera Arria V programmable device. All data and control processing functions are handled by the FPGA and its built-in NIOS CPU. Flash

memory is used to store and retrieve configuration information related to the various video formats that can be supported.
Controls can be implemented through a serial interface compatible with the USB 2.0 standard. These controls can be used to adjust display brightness, display gamma factor, display scan directions, as well as read back various status such as the microdisplay temperature.

4.2.1 Data input and control Functions

Figure 2: DisplayPort data formatting and decoding Figure 2 below shows a functional diagram of the DisplayPort data decoding. The DisplayPort data is first processed by an equalization circuit prior to being sent to the FPGA inputs as differential voltage pairs. The DisplayPort decoder (DP IP Block) handles the DisplayPort protocol and converts the input differential voltage signals into digital parallel data streams, along with extracting clock and synchronization information.
The NIOS CPU interfaces with the decoder to validate the video format and handle the display configuration data (EDID).

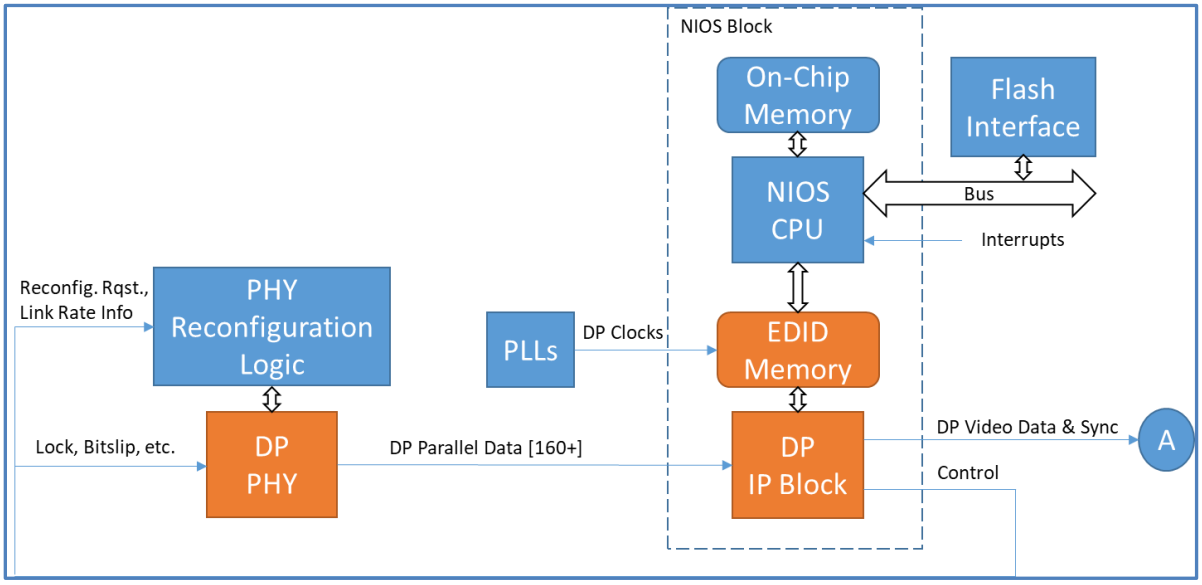

Figure 2: DisplayPort data formatting and decoding

4.2.2 Image data processing functions

Figure xx shows the data and format functions performed by the FPGA once the data has been converted to digital format
The system validates the input format not only from the header information present in the DisplayPort data stream but also by actual measurement of the vertical and horizontal synchronization signals, thereby ensuring maximum format integrity.
A multiline buffer is implemented to manage the DisplayPort flow without compromising the microdisplay operation. The maximum latency is less than one frame, even when using the minimum active window size afforded by the 2K x 2K Microdisplay.

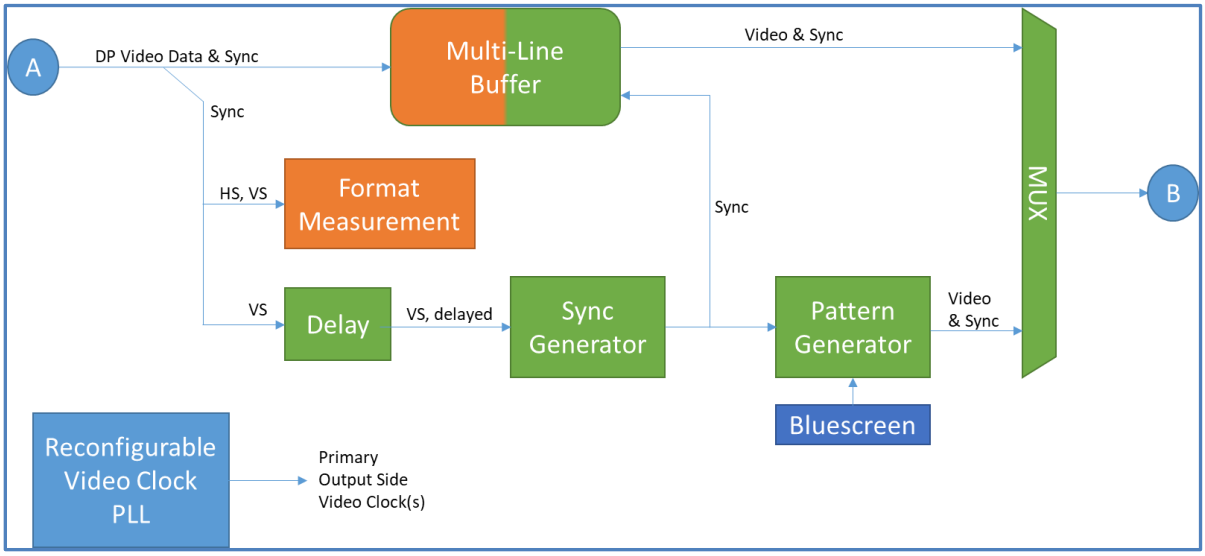

Figure 3: Digital Data Processing

An internal pattern generator is built into the FPGA that can be used for troubleshooting or display a fixed flat field pattern (Blue screen by default) when there is no valid video detected (either due to a lack of physical connection or an invalid data format).
A reconfigurable phase-locked loop clock generator handles the clock signals needed to output the lvds data to the microdisplay.

4.2.3 Output Data Formatting

Figure 4 shows the output data formatting function where the digital image data is formatted and converted to 18 lvds pairs as required by the 2K x 2K Microdisplay.

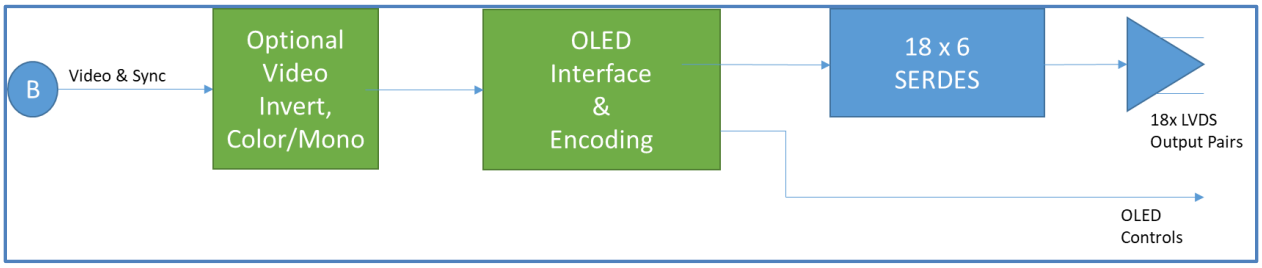

Figure 4: Display data output formatting

5. INPUT / OUTPUT DESCRIPTION

The 2K_CI has 5 connectors:

- Power Connector
- Data Connector
- Control Connector
- Microdisplay Connectors (2)

5.1 Power Connector

The power connector is a Molex Pico-Lock (PN# 503763-2) connector with positive side locks, and rated for 1.5A. A mating power cable is included with the 2K Compact Interface, and connects at its other end to a 9V DC power supply.

Pin#1: VIN DC Power input
Pin#2: GND Power return

5.2 Data Connector

The Data Connector is a USB-C physical connector whose pinout has been modified to map into the DisplayPort standard connections. Please note that although a USB-C connector is being used, this connector does not support the VESA DP Alt Mode on USB-C.
Figure 5 shows the wiring of the Data Connector of the interface.

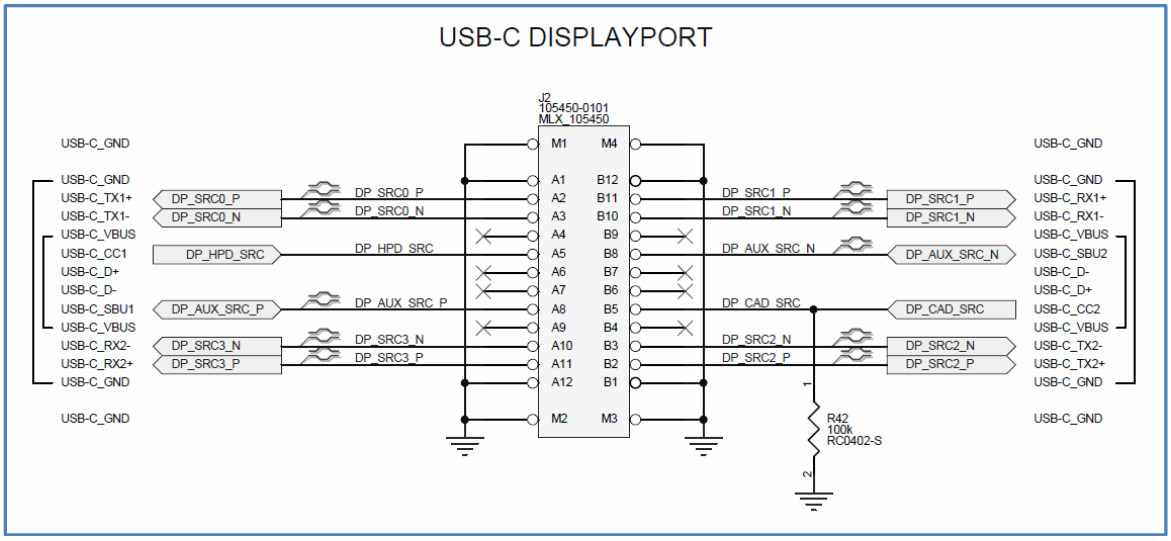

Figure 5: Data Connector Wiring

Physically, the connector is soldered onto the FPGA board such that the A side is facing up when looking at the FPGA board assembly from the side that carries the FPGA device.

The data cable provided with the 2K Compact Interface is a custom assembly. The USB-C end of the cable assembly has a mark on one side, which is the A side of the connector.

The electrical interface complies with the electrical requirements defined in the DisplayPort 1.2a VESA standard.

5.3 Control Connector

The 2K Compact Interface features a mini-USB connector, used to handle communication between the host and the interface for control purposes. The 2K CI interface supports the USB 2.0 standard. A USB A to mini-USB cable is provided with the 2K Compact Interface.

Figure 6 shows the connector wiring on the interface (industry standard wiring).

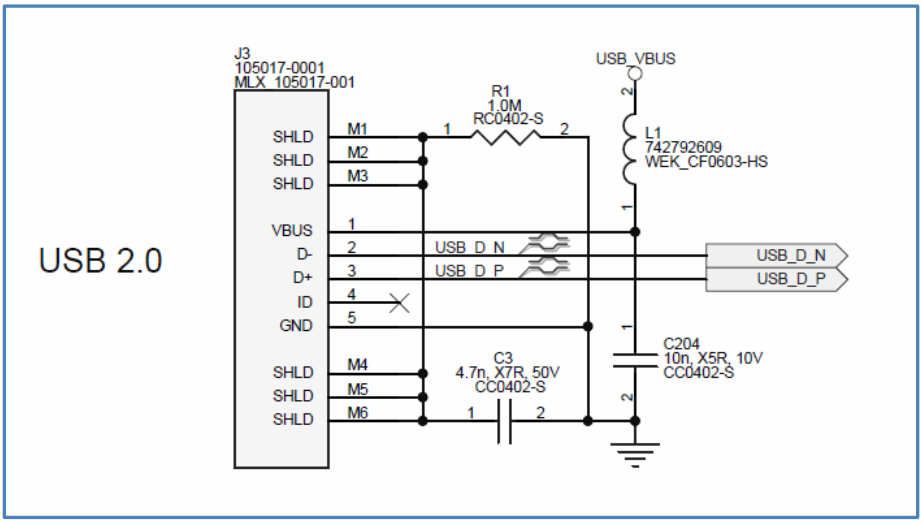

Figure 6: USB Connector

5.4 Microdisplay Connectors

Connector J4 – Hirose DF12B(3.0)-36DS-0.5V(81)

Pin #	Pin Name	Type	Description
1	RD5P	LVDS	LVDS Digital Data and Sync Input Port.
2	VDD1.8	Power	Input power for logic. (1.8V DC)
3	RD5N	LVDS	LVDS Digital Data and Sync Input Port.
4	VDD1.8	Power	Input power for logic. (1.8V DC)
5	GND	Power	Power return terminal.
6	VDD5.0V	Power	Input power for circuit (5.0V DC)
7	RD4P	LVDS	LVDS Digital Data and Sync Input Port.
8	VBUF	Power	Input power for Buffers (5.0V DC)
9	RD4N	LVDS	LVDS Digital Data and Sync Input Port.
10	VBUF	Power	Input power for Buffers (5.0V DC)
11	GND	LVDS	Power return terminal.
12	5VARY	Power	Input power for Pixel Array (5V DC).
13	RD3P	LVDS	LVDS Digital Data and Sync Input Port.
14	5VARY	Power	Input power for Pixel Array (5V DC).
15	RD3N	LVDS	LVDS Digital Data and Sync Input Port.
16	5VDC	Power	Input power for circuit (5.0V DC)
17	GND	LVDS	Power return terminal.
18	5VDC	Power	Input power for circuit (5.0V DC)
19	RD2P	LVDS	LVDS Digital Data and Sync Input Port.
20	GND	LVDS	Power return terminal.
21	RD2N	LVDS	LVDS Digital Data and Sync Input Port.
22	LVDS_ALIG	LVDS	LVDS Digital Data and Sync Input Port.
23	RESETB	LVDS	Asynchronous system reset (active low, 1.8V CMOS). 10K pull-up to 1.8V or external(user) control
24	BURNIN	Power	Burnin mode input (1.8V Active High)
25	RD1P	LVDS	LVDS Digital Data and Sync Input Port.
26	VPG	LVDS	-1.5 V DC Bias Input (Normal Operation) / +3.5V for Global Shutter operation
27	RD1N	LVDS	LVDS Digital Data and Sync Input Port.
28	GND	LVDS	Power return terminal.
29	GND	LVDS	Power return terminal.
30	VGN	Analog Out	Analog Output (0 to +1.8V) used for gamma calibration
31	RD0P	LVDS	LVDS Digital Data and Sync Input Port.
32	ENABLE	Logic In	Enable Logic Input (Used in Stereovision mode, 1.8V CMOS)
33	RD0N	LVDS	LVDS Digital Data and Sync Input Port.
34	VCOM	Analog Out	OLED Cathode Supply Output (0V to -6V)
35	GND	Power	Power return terminal.
36	SERADDR	Logic In	I2C Serial Port Device Address LSB (1.8V CMOS)

Connector J5 – Hirose DF12B(3.0)-40DS-0.5V(81)

Pin #	Pin Name	Type	Description
1	GND	Power	Power return terminal
2	GND	Power	Power return terminal
3	RD16N	LVDS	LVDS Differential Data Input Port
4	RD10N	LVDS	LVDS Differential Data Input Port
5	RD16P	LVDS	LVDS Differential Data Input Port
6	RD10P	LVDS	LVDS Differential Data Input Port
7	GND	Power	Power return terminal
8	GND	Power	Power return terminal
9	RD15N	LVDS	LVDS Differential Data Input Port
10	RD9N	LVDS	LVDS Differential Data Input Port
11	RD15P	LVDS	LVDS Differential Data Input Port
12	RD9P	LVDS	LVDS Differential Data Input Port
13	GND	Power	Power return terminal
14	GND	Power	Power return terminal
15	RD14N	LVDS	LVDS Differential Data Input Port
16	RD8N	LVDS	LVDS Sync input Port
17	RD14P	LVDS	LVDS Differential Data Input Port
18	RD8P	LVDS	LVDS Sync input Port
19	GND	Power	Power return terminal
20	GND	Power	Power return terminal
21	RD13N	LVDS	LVDS Differential Data Input Port
22	RCKP	LVDS	LVDS Differential Data Input Port
23	RD13P	LVDS	LVDS Differential Data Input Port
24	RCKN	LVDS	LVDS Differential Data Input Port
25	GND	Power	Power return terminal
26	GND	Power	Power return terminal
27	RD12N	LVDS	LVDS Differential Data Input Port
28	RD7N	LVDS	LVDS Differential Data Input Port
29	RD12P	LVDS	LVDS Differential Data Input Port
30	RD7P	LVDS	LVDS Differential Data Input Port
31	GND	Power	Power return terminal
32	GND	Power	Power return terminal
33	RD11N	LVDS	LVDS Differential Data Input Port
34	RD6N	LVDS	LVDS Differential Data Input Port
35	RD11P	LVDS	LVDS Differential Data Input Port
36	RD6P	LVDS	LVDS Differential Data Input Port
37	GND	Power	Power return terminal
38	GND	Power	Power return terminal
39	SDA	I/O	I2C Serial Port Data - Open Collector
40	SCL	Input	I2C Serial Port Clock

6. ELECTRICAL CHARACTERISTICS

Table 1 Absolute Maximum Rating

Symbol	Parameter	Min	Typ.	Max.	Unit
VIN	Input Power Supply	7		15	VDC
PD	VIN Power Dissipation			7	W
VBUS	USB Power Input			5.5	VDC
Tst	Storage Temperature	-55		+90	°C
Ta	Operating Temperature	-10		+70	°C
Vesd	Electrostatic Discharge – Human Body Model			±2000	V

Stresses at or above those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the following tables is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ.	Max.	Unit
VIN	Input Power Supply	7	9	12	VDC
VBUS	USB Power Input		5		VDC
Tst	Storage Temperature	-55		+90	°C
Ta	Ambient Operating Temp.	-10	+25	+70	°C

Table 3 AC Characteristics

Symbol	Parameter	Min	Typ.	Max.	Unit
Refresh Rate	2048 x 2048 Active Window	30	60	120	Hz
Pd VIN	Average Input Power Consumption (2K x 2K Mode 60 Hz refresh rate)		2.4(1)	2.7(1)	W
Ta	Ambient Operating Temperature	-10		+70	°C

(-10°C < Ta < +70°C, GND = 0V, VIN= +9.0V, VBUS = +5.0V)

(1) Interface alone, no microdisplay connected

Power consumption measured at 60 & 120Hz refresh rate, room ambient temperature and with a color image that represents an average video mode (See below Figure 7), with no microdisplay connected.

Figure 7: Typical Color Image

The table below is provided to illustrate the power consumption of the 2K_CI interface with a 2K x 2K color XL microdisplay running at ~ 100 cd/m2 luminance, for different frame rates and image contents. For these measurements, VIN = 9.0 VDC

Table 4 Interface + 2K x 2K Microdisplay Power Consumption

Image	Parameter	60Hz	85Hz	120Hz	Unit
Black Screen	VIN power consumption	2.45	2.55	2.74	W
White Screen	VIN power consumption	2.85	3.0	3.33	W
Color Image (see Fig 7)	VIN power consumption	2.91	3.2	3.47	W

6.1 Timing Characteristics

The timing information provided below relates to the frame and line timing, not the LVDS physical interface (described in section 9.1.1.2 below))

6.1.1 Video Formats and Timing

The following video formats are supported by default by the 2K_CI

- 2048 x 2048 @ 60Hz, 85Hz or 120Hz
- 1920 x 1200 @ 60Hz, 85Hz or 120 Hz
- 1920 x 1080 @ 60Hz, 85Hz or 120 Hz
- 1280 x 1024 @ 60Hz, 85Hz or 120 Hz

Additional formats can be configured, depending on the flexibility of the source system.

The 2K_CI interface timing is compliant with the DisplayPort Standard version 1.2a

7. CONTROL INTERFACE

7.1 Serial Interface Protocol

The 2K_CI interface has controls that can be accessed using the USB compatible serial interface. It supports ASCII communications and can operate as a virtual serial port

Port configuration:

- 8 bits
- No parity
- 1 stop bit
- No flow control
- Speed: 921,600 bauds

7.2 Control Commands

Table 5 below lists the command available to set interface and display parameters as well as store/retrieve interface formats

Table 5: Serial Interface Commands

Command	Description	Argument			
		Type	Min	Default	Max
BLUESCRN	24-bit RGB color value for "blue" screen which is displayed when no input video is available - each value 0~0xff - bits [23:16] = red - bits [15:8] = green - bits [7:0] = blue - default value = 0x000055	UINT32	0	0x55	0xffffff
BRT	Set brightness (luminance)	UINT16	0	0x0A	BRTMOD
BRTDEC	Decrement BRT by 1	None	-	-	-
BRTDFLT	Command resets brightness to the original hardware default value	None	-	-	-
BRTINC	Increment BRT by 1	None	-	-	-
BRTLPC	Display Linear Perception Coeffecient - range 0.5 ~ 5.0 - default 2.5	float	0.5	2.5	5.0
BRTMOD	Set number of BRT adjustment steps (modulus)	UINT16	0	16	256
DCFG	Delete manually saved configuration data from Flash	None	-	-	-
DDYN	Delete dynamically saved configuration data from Flash	None	-	-	-
DIMCTL	Direct access to OLED DIMCTL register	BYTE	0	-	127
DP130D	Access to SN75DP130 DisplayPort Configuration Data (DPCD) registers, indexed as: 0: 0x00100 link bw set 1: 0x00101 lane count set 2: 0x00103 train lane0 set 3: 0x00104 train lane1 set 4: 0x00105 train lane2 set 5: 0x00106 train lane3 set 6: 0x0010F train lane0 1 set2 7: 0x0110F train lane2 3 set2 8: 0x00600 set power	BYTE	0	-	0xff
DP130R	Direct access to SN75DP130 I2C registers	BYTE	0	-	0xff
DPCD	Access to Bitec DPCD register set	BYTE	0	-	0xff
DPDC	Display Persistence Duty Cycle (1~100)	BYTE	1	100	100
DPEQ	Sets equalization value in DP130, for all lanes: 0 = 0 dB 1 = 3.5 dB 2 = 6 dB 3 = 8 dB 4 = 10 dB 5 = 13 dB (dflt) 6 = 15 dB 7 = 18 dB Change occurs immediately	BYTE	0	-	7

Command	Description	Argument			
		Type	Min	Default	Max
DPLQA	Enable/disable LQA 0=disable 1=enable Will be applied at the next DPRST or received video format change	BOOL8	0	1	1
DPREG	Access to Bitec internal register set	UINT32	0	-	0xffffffff
DPRST	Reset DisplayPort receiver 0=restart only (no DP130 initialization) 1=full reset	BYTE	0	-	1
DPSQLCH	Sets receiver squelch level: 0 = 40 mVpp 1 = 80 mVpp 2 = 160 mVpp 3 = 250 mVpp 4 = disabled (dflt) Change occurs immediately	BYTE	0	4	4
DPSTAT	Prints DisplayPort detailed receive status (debug)	None	-	-	-
EDID	Dumps the contents of the EDID image to the serial port	BYTE	0	-	4
EDIDCURR	Displays the number/index of the internal EDID file currently in use by the DisplayPort interface. This can be different to the EDIDSEL number if for any reason there was an error loading the file requested by the EDIDSEL command (for example, if the requested file had not been programmed). Please see the EDID command for more information.	BYTE	-	-	-
EDIDPROG	Invokes YMODEM to program EDID file to Flash	BYTE	1	-	4
EDIDSEL	Selects the EDID image to use. The DP interface is reset after a change so that the host will see the new data.	BYTE	0	0	4
F 0	Queries Flash Prom type	BYTE	0	-	1
FEDBG	Causes debug serial "printout" of 9 different debug counters attached to the video format detection algorithm	None	-	-	-
GAMMA	Gamma value for OLED - floating point - range 0.001 thru 9.999 accepted	float	0.001	1.8	9.999
HPOS	Set horizontal image position offset: 0 = default center neutral	NT16	-2047	0	+2047
HSCAN	Display horizontal scan direction (0=L->R; 1=R->L)	BYTE	0	0	1

Command	Description	Argument			
		Type	Min	Default	Max
I2CA	I2C Debug Address - to be set up prior to sending I2CC command - 32-bit word format: 76543210 (hex digits, not bits) ======== bbddssss | | |____ ssss = subaddr | |_____ dd = dev addr |_____ bb = busnum	UINT32	0	-	0xffffffff
I2CC	I2C Debug Command - bus activity takes place when this is written - 16-bit word format: 3210 (hex digits, not bits) ==== txcc || |__ cc = bytecount minus 1 ||____ x = command (0=wr, 1=rd, 3=rd w/stop) |_____ t = subaddr type (0=none, 1=8b, 2=16b, 3=test)	UINT16	0	-	0xffff
I2CD	I2C Debug Data - up to 16 bytes, indexed - for I2C writes: set up prior to sending I2CC command - for I2C reads: read back after sending I2CC command	BYTE	0	-	0xff
IDRF	Direct access to OLED IDRF register	BYTE	0	200	0xff
IVQ	Query input video returns lock status, vert & horiz resolution & frequencies	None	-	-	-
LEDEN	Set on-board LED enable: 0 = BLU, RED LEDs disabled 1 = BLU, RED LEDs enabled	BOOL8	0	1	1
LIST	Prints unsorted, unordered list of all available commands	None	-	-	-
LUTM	Gamma LUT control: 0=Off 1=Gamma Only 2=VGN Only 3=Gamma and VGN	BYTE	0	3	3
MAXLUM	Set maximum display luminance, 100% = display device upper limit - minimum value = 10	BYTE	10	100	100
MEAS	Causes debug serial "printout" of most recent measurements of input video format - includes H-Active, H-Total V-Active, V-Total, fV (Hz), fH (KHz), fP (MHz) - measurements in the H direction may appear to be incorrect due to the use of an intermediate clock which is not running at the usual pixel rate	None	-	-	-

Command	Description	Argument			
		Type	Min	Default	Max
MINLUM	Set minimum display luminance, 0% = display device lower limit	BYTE	0	0	99
NOPIXDBL	Option to inhibit automatic OLED pixel doubling when the received input video format is small enough to allow doubling (i.e. less than or equal to 1/2 of the OLED image size in each direction) 0 = doubling permitted 1 = doubling inhibited	BOOL8	0	0	1
OGAMTBL	OLED returns register values which have been transferred to interpolator . .	UINT16	-	-	-
OGSPFRM	Global shutter on-time expressed as a percentage of the frame period - only this on-time value is saved - if not changed by user it remains constant across video format changes - shutter on-time is always centered at the center point of vertical blanking	float	0.006	5	99.994
OGSPVBL	Global shutter on-time expressed as a percentage of the vertical blanking period - this value will be converted to/from the OGSPFRM value - note that such conversions are dependent on the current video format - a readback of OGSPVBL will (most likely) change when the video format changes	float	Must satisfy OGSPFRM "arg min" after conversion	-	Must satisfy OGSPFRM "arg max" after conversion
OGSUSEC	Global shutter on-time expressed as microseconds - this value will be converted to/from the OGSPFRM value - note that such conversions are dependent on the current video format - a readback of OGSUSEC will (most likely) change when the video format changes	UINT32	Must satisfy OGSPFRM "arg min" after conversion	-	Must satisfy OGSPFRM "arg max" after conversion
OGSEN	Global shutter enable/disable 0 = disable (dflt) 1 = enable	BOOL8	0	0	1
OHACTMIN	Adjusts or reads back the minimum number of pixels in the horizontal active period to be used by the OLED.	UINT16	-	-	-
OLED	Direct access to OLED I2C registers	BYTE	0	-	0xff
OLEDBI	Enable/disable internal OLED test pattern: 0: Burn-in (all white) 1: Color Bar 2: 16 level gray scale 3: Checker Board 4: Vertical Line 5: Horizontal Line 6: Grid Pattern 7: Off	BYTE	0	0	7

Command	Description	Argument			
		Type	Min	Default	Max
OLEDRESET	Command sequences OLED shutdown followed by re-startup	None	-	-	-
ORUNST	Current running status of OLED softeware (debug) 0 = Idle 1 = Power On Pending 2 = Startup Delay 3 = Run 4 = Reset Delay 5 = Power Off Pending Note: In this design only the "Idle" and "Run" states are likely to be seen.	BYTE	-	-	-
OSLEEP	Directly controls OLED "All System Power Down" bit	BOOL8	0	0	1
OTEMP	Query OLED Temperature	float	-	-	-
OVACTMIN	Adjusts or reads back the minimum number of lines in the vertical active period to be used by the OLED.	UINT16	-	-	-
PATT	Set OLED Driver Test Pattern: 0 = No pattern 1 = Lines (W on B) 2 = Color Bars 100% 3 = Color Bars 75% 4 = Gray scale (L => R: B => W) 5 = Gray scale (L => R: W => B) 6 = Gray ramp (L => R: B => W)	BYTE	0	0	7
PATTLO	Optionally splits the pattern display into two parts - the upper 2/3 is set up by the PATT command - the lower 1/3 is set up by this PATTLO command - uses the same values as the PATT command - setting this to zero (no pattern) disables the split - only effective when PATT is non-zero	BYTE	0	0	7
POWER	Power control: 0 = Off 1 = On 2 = Auto: power down after timeout (see TIMEOUTSEC)	BYTE [3:0]	0	2	2

Command	Description	Argument			
		Type	Min	Default	Max
QPOS	Specially timed command, combining HPOS and VPOS values - the resulting OLED LFTPOS, RGTPOS, TOPPOS and BOTPOS register values are combined and transmitted to the OLED in a single message - the message is timed so as not to straddle the leading edge of vertical sync, which is where the OLED internally transfers the "POS" register values to working registers - in other words, if the QPOS command is received too late in a frame to meet this requirement, then software will wait until the following frame starts before transmitting the message to the OLED - syntax of the data is unusual, in that it is a 32-bit word which consists if two signed 6-bit words, with the HPOS value in the upper 16 bits, and the VPOS value in the lower 16 bits - for example, if HPOS=VPOS=34 (decimal), the command is "QPOS 0x00220022" - signed values are trickier - for example, if HPOS=VPOS=-64, send "QPOS 0xFFC0FFC0"	UINT32	Each 16-bit value: -2047	-	Each 16-bit value: +2047
RCFG	Recall manually saved configuration data from Flash	None	-	-	-
RDYN	Recall dynamically saved configuration data from Flash	None	-	-	-
SCFG	Save configuration data to Flash	None	-	-	-
TIMEOUTSEC	In the absence of a video signal at the input, the OLED will be powered down after this timeout period, expressed in seconds - this behavior must be enabled by the POWER command being set to Auto	UINT16	0	0x12C	0xffff
UPDATE	Invokes YMODEM to progrram FPGA boot-image to Fpash	None	-	-	-
VER	Causes serial "printout" of the current FPGA and software versions - for example: FW+SW C008-1300-01 FW C008-1200-01 Ver 110 SW C008-1000-01 Ver C008 2Kx2K RGB Driver v0.11, 06/22/2018	None	-	-	-
VGNDLY	Minimum delay between VGN updates - unit = milliseconds - default = 5000	UINT16	0	0x1388	0xffff
VGNGCT	Readback calculated gamma table coefficients ("GC" values)	float	-	-	-
VGNT	Most recent VGN voltages	float	-	-	-

Command	Description	Argument			
		Type	Min	Default	Max
VGNV	Direct and immediate read of VGN voltage	float	-	-	-
VIDINFO	Video format values in current use (input side), indexed: 0: H Total 1: H Active 2: H Begin 3: V Total 4: V Active 5: V Begin 6: valid (internal flag)	UINT16	0	-	Format values: 4095
VIDINV	Set video inversion mode: 0 = normal 1 = video inverted (B <=> W)	BYTE	0	0	1
VPOS	Set vertical image position offset: 0 = default center neutral	INT16	-2047	0	+2047
VSCAN	Display vertical scan direction (0=T->B; 1=B->T)	BYTE	0	0	1

8. MECHANICAL CHARACTERISTICS

Power Connector

Manufacturer	Molex
Manufacturer Part Number	503763-2

Data Connector

Manufacturer	Molex
Manufacturer Part Number	1054450-0101

Control Connector

Manufacturer	Molex
Manufacturer Part Number	105017-0001

Connector J4

Manufacturer:	Hirose
Manufacturer Part Number:	DF12A(3.0)-36DS-0.5V(81)

Connector J5

Manufacturer:	Hirose
Manufacturer Part Number:	DF12A(3.0)-40DS-0.5V(81)

Weight:	48 grams (including mounting feet and hardware)
Printed Circuit Board Material:	FR4
Printed Circuit Board Tolerances:	± 0.2 mm (both axes)
Heat Spreader Material	Aluminum

A CAD model (STP format) is available upon request.

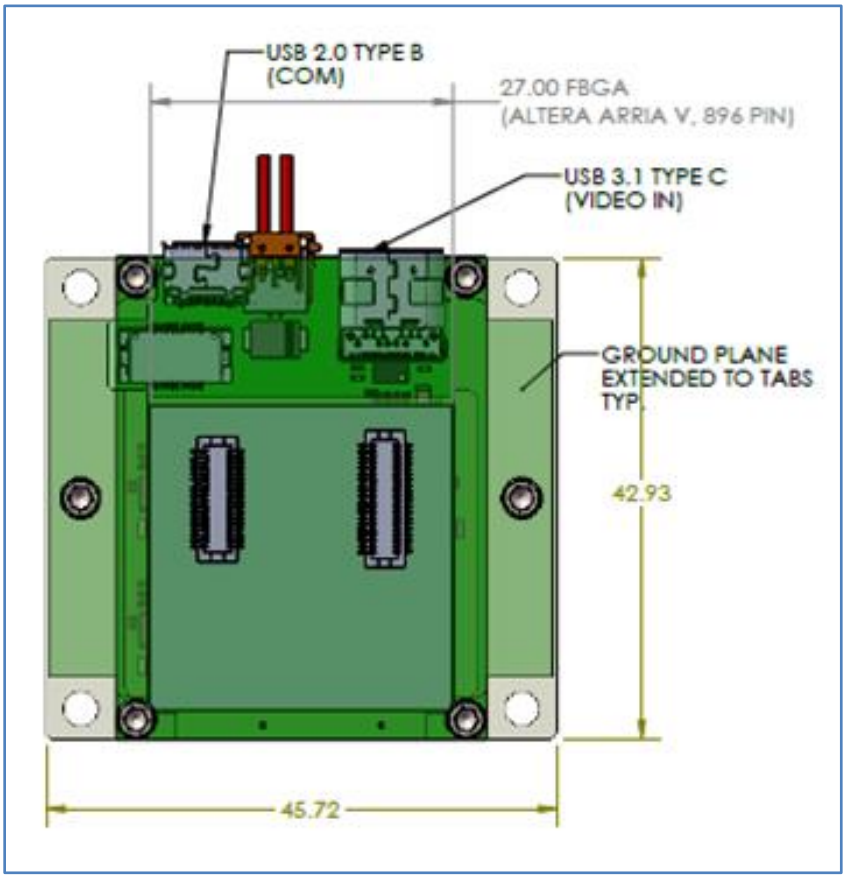

Figure 8: Interface top view (Dimensions in mm)

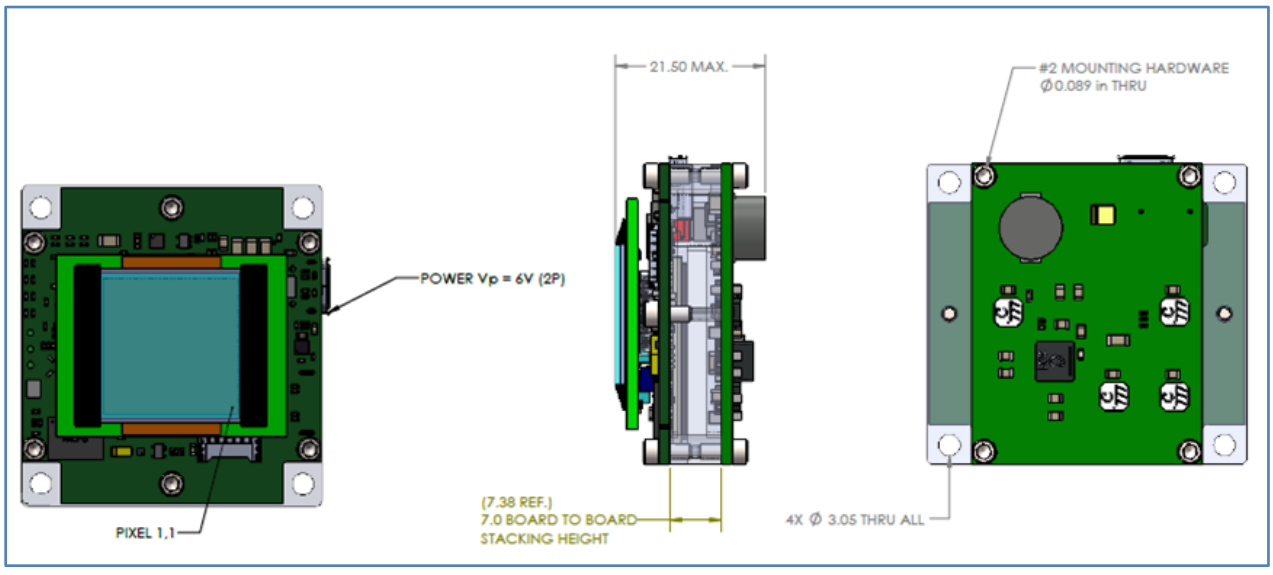

Figure 9: Interface top, side and bottom views