2K X 2K

2048 X 2048 RECONFIGURABLE COLOR XL AMOLED MICRODISPLAY

DATASHEET
Rev A

For Part Numbers:

EMA-101306-01

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Revision Level	ECN	Date	Scope
-		Feb. 2018	Initial Release
A	000649	Jan 2019	Update assembly view – rear side p22 Updated Connector J1 pin description p11 Updated eeprom address p42

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1. MAIN FEATURES

- 27.25 mm (1.07”) diagonal 2072 x 2072 color microdisplay
- 9.3 micron color pixel
- OLED XL technology: up to 250 cd.m^{-2} luminance (@ 25°C) and 100,000:1 contrast ratio
- Up to 10,000: 1 dimming ratio (at maximum luminance)
- User configurable, gamma correction over brightness and temperature
- Automatic, user adjustable, brightness control over brightness and temperature
- Adjustable active window size (512x512 up to 2072x2072 pixels) and location
- Pixel doubling mode
- Power consumption scalable with active window size
- Rolling shutter mode
- Global shutter mode
- 120 Hz refresh rate (full screen mode) up to ~ 500 Hz (512 x 512 active window mode)
- Flexible, FPGA compatible LVDS data/timing interface
- Serial port (I2C) configurable integrated register table
- Wide operating temperature range: -45°C to +70°C

2. GENERAL DESCRIPTION

The 2Kx2K Reconfigurable Color OLED-XL (2K_CFXL) device from eMagin Corporation is an active-matrix organic light emitting diode (AMOLED) microdisplay intended for near-to-eye applications that demand high brightness, high resolution, high image quality, compact size, and low power. Combining a total of 12,879,552 active dots, the 2K_CFXL display is built on a single crystal silicon backplane and features eMagin's proprietary thin-film OLED XL technology offering extended life and luminance performance.

The active array is comprised of 2072 x 2072 square color pixels with a 9.3-micron pitch and a 75% fill factor. An extra 24 columns and 24 rows (beyond the 2048 x 2048 main array) are provided to enable the 2K_CFXL display to be shifted by steps of 1 pixel in the X and Y directions for optical alignment purposes. Each full pixel is laid out as three 3.1 x 9.3 micron identical sub-pixels, which together form the 9.3-micron square RGB color group. Three primary color filter stripes are applied in alignment with the sub-pixels on a white-emissive OLED layer to form the color display.

Unique to this microdisplay is the ability to configure the active area to any size from 512 x 512 up to 2048 x 2048 pixels in steps of four columns and one row. The resulting window can be positioned anywhere within the underlying 2072 x 2072 pixel array. The display timing can be adjusted to match the format being shown, enabling lower power operation due to the reduced pixel bandwidth, similar to that of smaller display having the same format. The number of data inputs can also be reduced based on the format selected, allowing for a smaller interface interconnect to be used for some applications.

The 2K_CFXL design features eMagin's proprietary "Deep Black" architecture that ensures off- pixels are truly black, automatically optimizes contrast under all conditions, and delivers improved pixel uniformity. In addition to its flexible matrix addressing circuitry, the 2K_CFXL includes the same automatic internal brightness control function implemented on other eMagin microdisplay products. Gamma correction over temperature and brightness changes is enabled by a direct OLED sensor feedback output that can be used by the host system to set a wide range of gamma correction profiles.
Two independent functions are also provided to minimize motion artifacts:

- A pulse width modulation (PWM), also known as a rolling shutter mode that can also be used for display brightness adjustment
- A global shutter mode whereby the array is turned on all at once for a programmable period of time.

The 2K_CFXL includes a very low-power, low-voltage-differential-signaling (LVDS) serialized interface for video data transport that minimizes the number of board interconnections and connector size, reduces electromagnetic emissions (EMI), and enables a lightweight and flexible cable link to a remote video source. Compatibility with standard LVDS drivers found in most commercially available FPGAs simplifies the system integrators task.

Detailed device specifications and application information for the 2K_CFXL microdisplay produced by eMagin Corporation are provided in this document.

3. FUNCTIONAL OVERVIEW

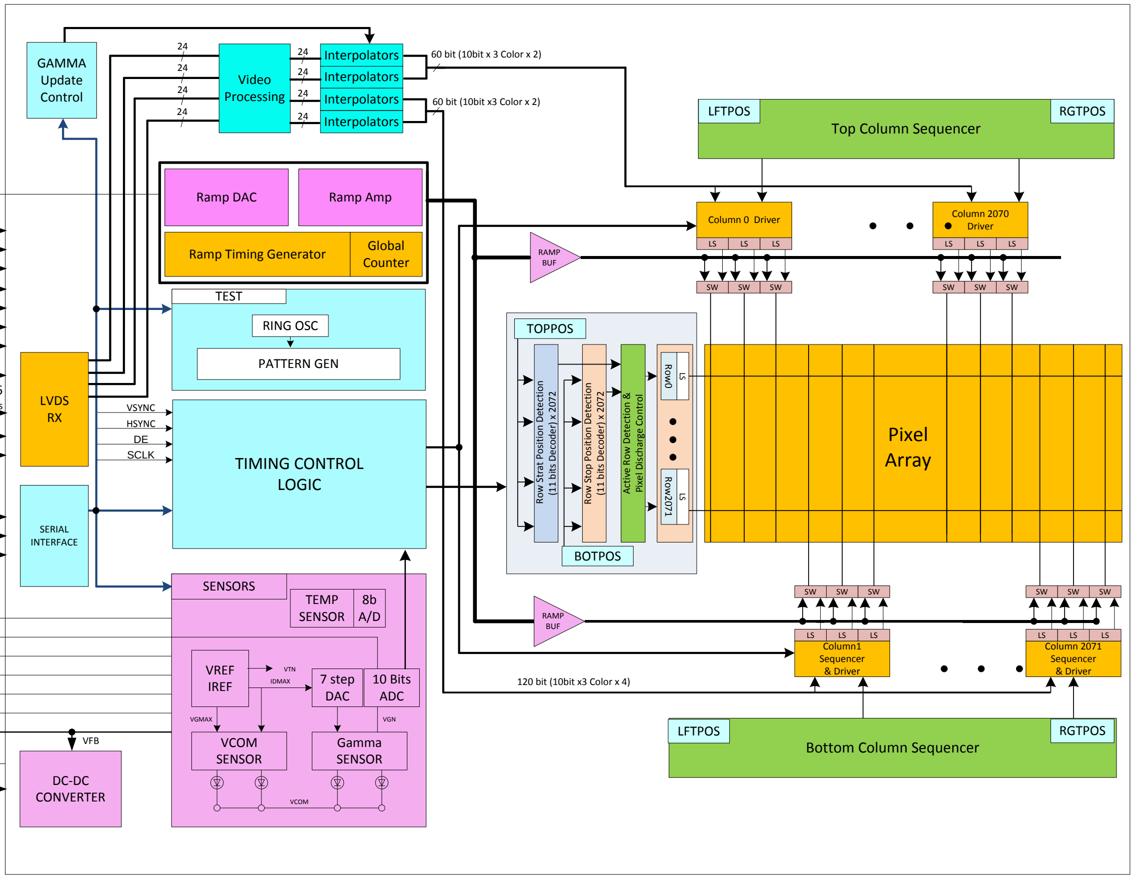


Figure 1: Top-level block diagram for 2K_CFXL

The 2K microdisplay includes multiple functions that allow the display to be operated with minimal supporting hardware, similar to a typical flat panel monitor. The functions include, data control interface, format and timing control, gamma correction, brightness control, active matrix drivers, on-chip power converter, temperature sensor, power consumption management, serial port interface, and built-in pattern generator.

Following is a high-level description of each major function. Details can be found further down in this document.

Data Control Interface

The data and control interface uses a 6-bit custom serialization Low Voltage Differential Signaling protocol (LVDS) that is hardware compatible with commonly available FPGA (Field Programmable Gate Array) devices. The custom nature of the eMagin interface lies in the use of a separate clock pair, which eliminates the need for a power consumption intensive on-chip clock recovery circuit.

The 2K microdisplay LVDS interface has been designed for flexibility in that depending on the format implemented, refresh rate used and/or colors used, a subset of the available LVDS pairs can be used, thereby reducing interconnect requirements at the system level. Configurations using 5, 9 or 17 data pairs are possible. These correspond to 1, 2 or 4 pixels per input clock cycle.
The 2K microdisplay supports a custom 6-bit serial interface and the LVDS interface converts the input serial data stream into four parallel data channels that are routed to the gamma correction circuit prior to being used by the active matrix column drivers.
eMagin Corporation makes available to its customers the host-side FPGA source code needed to implement a fully functional LVDS interface including skew compensation.

Format and Timing Control

Through the on-chip register table, the 2K microdisplay can be configured over a wide range of active window formats, from 512 x 512 pixels up to full screen. The architecture implementation allows the host system to adjust its timing (pixel clock and refresh rate) to the size of the configured window: only the active pixels are being driven, the rest of the array is internally driven to black without any timing penalty or overhead.
A reduction of the active window therefore enables a higher refresh rate to be used, the upper limit being controlled by the maximum supported LVDS clock frequency (430 MHz).
An additional feature of the 2K microdisplay is the possibility to locate the active window anywhere within the underlying 2072 x 2072 pixel array. A further capability of the display is the ability to update the location of the active window frequently (minimum update rate is 16ms), using dedicated registers accessible through the serial port.
The scan direction is also programmable in both directions.
Finally a pixel doubling function is included that replicates an input pixel over four (4) active matrix pixels. Thus, a 1K x 1K source input can be mapped to the full 2K x 2K active window directly using a dedicated on-chip register accessible through the serial port.

Gamma Correction

The 2K microdisplay pixel response is non-linear, requiring the use of an internal gamma correction circuit.
The gamma correction circuit is based on a real time 8-point linear interpolator, which can be configured via dedicated registers to adjust the desired gamma of the display.
The 8 points are calculated externally by the host system.
An internal sensor allows the display response to be captured and used to generate the eight (8) points needed by the interpolator. It can be used in real time. As a result, no prior calibration is required to ensure the desired gamma will be available to the user. Should the need arise, it is also possible to configure the 8 gamma coefficients manually via the register interface
Each color channel can be configured independently.

Brightness Control

The 2K microdisplay brightness is set using a primary register (IDRF) and a secondary register (DIMCTL) that modulates the IDRF setting from 0% to 128% of the brightness level determined by the IDRF value.
This control is referred to as the analog brightness (or luminance) control. A large dimming ratio is achievable using these two registers in combination, typically over 2,000:1

A dedicator on-chip sensor provides a regulation mechanism that maintains the luminance setting regardless of image content and over the entire operational temperature range (within 10%). Factory calibration provides a means to set the absolute luminance of the microdisplay and is based on the linear proportionality of luminance with the IDRF register value. The slope and intercept values of each microdisplay is measured at the factory and saved in the on-board eeprom. As a result, binocular applications can readily use any 2K microdisplay without additional calibration to get matching luminance response from each microdisplay.

In addition, a pulse width modulation (PWM) function is available to control luminance (digital luminance control) that sets the amount of time a pixel row is turned on, on a row time basis. This technique is also known as the rolling shutter dimming. Dedicated registers are used to program the “on-time” of pixel rows, which can then be used to adjust the overall display luminance.
The rolling shutter function also provides for reduced motion artifacts by allowing the image to turn off prior to the next frame update. This is similar to the behavior of CRT displays where the phosphor grains are illuminated briefly and decay afterwards, leaving no impression on the retina before the next video frame is displayed. As a result, motion across the display screen is perceived as smooth as opposed to “jumpy”.

Support for global shutter mode has been implemented in the 2K microdisplay that allows the image to be displayed only after the entire frame has been loaded into the pixel array. An analog input (VPG) can be used to turn on/off the array once all pixels have been updated. A custom host timing is required to provide enough blanking time after the frame data has been loaded to turn the display on, prior to loading the next frame. The on-time duration provides another method to control luminance but the main reason for using the global shutter mode is the elimination of any motion artifact.

Active Matrix Drive
The 2K microdisplay uses a voltage programmed pixel cell. Pixels are programmed on a line-by-line basis. The voltage, which has been gamma corrected, is generated using a sampled ramp architecture that relies on an internal 10-bit DAC (Digital to Analog Converter) and digital comparators at each column that set the voltage levels to be programmed into the pixels.
The column drive is split between top and bottom drivers, each having two 10-bit data busses. Data is loaded sequentially into digital column registers during one line period. The registered data is transferred to the comparators, and subsequently to the selected pixel row, during the next line period. As a result, there is a 2-line period pipeline delay between data being clocked into the display and data being displayed.
The row and column scanners can be programmed for scan direction as well as for starting and ending rows/columns. Unused pixels are automatically reset to black every frame.

On-chip Power Converter
The OLED current-voltage (IV) characteristic has a wider voltage range that can be handled by the 5-Volt capability of the microdisplay CMOS backplane. As a result, a negative power supply rail capability is required for normal operation.
It is also necessary to control the negative voltage in order to maintain consistent luminance over time.

The 2K microdisplay component incorporates a negative dc-dc converter using a combination of discrete components mounted on the rear side of the component and digital control built into the CMOS backplane. The implementation enables a closed loop control that also relies on an internal sensor to maintain luminance not only over time but also over temperature in an automated manner.
There is no direct user-accessible control of the converter, its operation is based on the values written to the IDRF and DIMCTL registers.

Temperature Sensor
The 2K microdisplay includes an on-chip temperature sensor that is used by the automatic gamma correction function and can also be accessed through the serial interface. The sensor is factory calibrated and the calibration factors are saved in the on-board eeprom for each microdisplay. Additionally, the sensor can be manually calibrated by the user if need be.

Power Consumption Management
The different functional blocks in the 2K microdisplay can be disabled by turning their power rails off. This is achieved through two power-down registers (ANAPWRDN1, ANAPWRDN2). Power consumption can therefore be controlled during idle times to minimize overall battery drain when the display is used in mobile applications.

Serial Interface
Access to the on-chip register is implemented with an industry standard slave-mode only I2C bus that can operate up to 400 KHz. The least significant bit of the display address is configurable (high or low) to allow for binocular operation. The device address has been selected to avoid conflict with typical I2C bus devices such as memory and or controller circuits.
The open-drain data (SDA) and input clock (SCL) lines can be operated from +1.8V up to 5V.
The 2K microdisplay configuration is based on a set of internal registers that can be used to setup every major function available to the user.
The 2K CMOS backplane has no permanent storage capability. As a result, the internal registers must be reconfigured whenever the display power is cycled. Default values are built into the backplane that will prevent any damage to occur but will not enable display operation.
By default, when the display power is turned on, there will be no image displayed until the DISPOFF bit in the DISPMODE register (bit 7) is set to 0. This provides the host system full control over what is or is not displayed at power on.

The 2K microdisplay component includes an on-board eeprom (256 locations) mounted on the rear side of the assembly. The eeprom, which is also accessible using the I2C serial port, contains information specific to the microdisplay including, serial number, factory calibration data and register values for the typical performance measured during factory acceptance testing. A typical use of the eeprom is to read the register values at power on, write them to the microdisplay and then turn the DISPOFF bit off to allow the display to function.

Pattern Generator
A programmable on-chip pattern generator is available to the user. Basic monochrome and color patterns can be displayed when the generator is enabled by setting the PATTEN bit (bit 3) in register TPMODE (register 14h).

4. INPUT / OUTPUT DESCRIPTION

Two connectors are required for display operation.

Connector J1 – Hirose DF12D(0.3)-36DP-0.5V(81)

Pin #	Pin Name	Type	Description
1	RD5P	LVDS	LVDS Digital Data and Sync Input Port.
2	VDD1.8	Power	Input power for logic. (1.8V DC)
3	RD5N	LVDS	LVDS Digital Data and Sync Input Port.
4	VDD1.8	Power	Input power for logic. (1.8V DC)
5	GND	Power	Power return terminal.
6	VDD5.0V	Power	Input power for circuit (5.0V DC)
7	RD4P	LVDS	LVDS Digital Data and Sync Input Port.
8	VBUF	Power	Input power for Buffers (5.0V DC)
9	RD4N	LVDS	LVDS Digital Data and Sync Input Port.
10	VBUF	Power	Input power for Buffers (5.0V DC)
11	GND	LVDS	Power return terminal.
12	5VARY	Power	Input power for Pixel Array (5V DC).
13	RD3P	LVDS	LVDS Digital Data and Sync Input Port.
14	5VARY	Power	Input power for Pixel Array (5V DC).
15	RD3N	LVDS	LVDS Digital Data and Sync Input Port.
16	5VDC	Power	Input power for circuit (5.0V DC)
17	GND	LVDS	Power return terminal.
18	5VDC	Power	Input power for circuit (5.0V DC)
19	RD2P	LVDS	LVDS Digital Data and Sync Input Port.
20	GND	LVDS	Power return terminal.
21	RD2N	LVDS	LVDS Digital Data and Sync Input Port.
22	LVDS_ALIG	LVDS	LVDS Digital Data and Sync Input Port.
23	RESETB	LVDS	Asynchronous system reset (active low, 1.8V CMOS). 10K pull-up to 1.8V or external(user) control
24	BURNIN	Power	Burnin mode input (1.8V Active High)
25	RD1P	LVDS	LVDS Digital Data and Sync Input Port.
26	VPG	LVDS	-1.5 V DC Bias Input (Normal Operation) / +3.5V for Global Shutter operation
27	RD1N	LVDS	LVDS Digital Data and Sync Input Port.
28	GND	LVDS	Power return terminal.
29	GND	LVDS	Power return terminal.
30	VGN	Analog Out	Analog Output (0 to +1.8V) used for gamma calibration
31	RD0P	LVDS	LVDS Digital Data and Sync Input Port.
32	ENABLE	Logic In	Enable Logic Input (Used in Stereovision mode, 1.8V CMOS)
33	RD0N	LVDS	LVDS Digital Data and Sync Input Port.
34	VCOM	Analog Out	OLED Cathode Supply Output (0V to -6V)
35	GND	Power	Power return terminal.
36	SERADDR	Logic In	I2C Serial Port Device Address LSB (1.8V CMOS)

Connector J2 – Hirose DF12D(0.3)-40DP-0.5V(81)

Pin #	Pin Name	Type	Description
1	GND	Power	Power return terminal
2	GND	Power	Power return terminal
3	RD16N	LVDS	LVDS Differential Data Input Port
4	RD10N	LVDS	LVDS Differential Data Input Port
5	RD16P	LVDS	LVDS Differential Data Input Port
6	RD10P	LVDS	LVDS Differential Data Input Port
7	GND	Power	Power return terminal
8	GND	Power	Power return terminal
9	RD15N	LVDS	LVDS Differential Data Input Port
10	RD9N	LVDS	LVDS Differential Data Input Port
11	RD15P	LVDS	LVDS Differential Data Input Port
12	RD9P	LVDS	LVDS Differential Data Input Port
13	GND	Power	Power return terminal
14	GND	Power	Power return terminal
15	RD14N	LVDS	LVDS Differential Data Input Port
16	RD8N	LVDS	LVDS Sync input Port
17	RD14P	LVDS	LVDS Differential Data Input Port
18	RD8P	LVDS	LVDS Sync input Port
19	GND	Power	Power return terminal
20	GND	Power	Power return terminal
21	RD13N	LVDS	LVDS Differential Data Input Port
22	RCKP	LVDS	LVDS Differential Data Input Port
23	RD13P	LVDS	LVDS Differential Data Input Port
24	RCKN	LVDS	LVDS Differential Data Input Port
25	GND	Power	Power return terminal
26	GND	Power	Power return terminal
27	RD12N	LVDS	LVDS Differential Data Input Port
28	RD7N	LVDS	LVDS Differential Data Input Port
29	RD12P	LVDS	LVDS Differential Data Input Port
30	RD7P	LVDS	LVDS Differential Data Input Port
31	GND	Power	Power return terminal
32	GND	Power	Power return terminal
33	RD11N	LVDS	LVDS Differential Data Input Port
34	RD6N	LVDS	LVDS Differential Data Input Port
35	RD11P	LVDS	LVDS Differential Data Input Port
36	RD6P	LVDS	LVDS Differential Data Input Port
37	GND	Power	Power return terminal
38	GND	Power	Power return terminal
39	SDA	I/O	I2C Serial Port Data - Open Collector
40	SCL	Input	I2C Serial Port Clock

5. ELECTRICAL CHARACTERISTICS

Table 5-1 : Absolute Maximum Ratings

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD1.8	Front End Power Supply	-0.3		2.5	VDC
VDD5	Array/Analog Power Supply	-0.3		5.5	VDC
VCOM	Common electrode bias	-6		0	VDC
VPG	Array Bias Supply	-3	-1.5	0	VDC
VI	Input Voltage Range	-0.3		VDD+0.3	VDC
VO	Output Voltage Range	-0.3		VDD+0.3	VDC
PD	Power Dissipation			1	W
Tst	Storage Temperature	-55		+90	°C
Ta	Operating Temperature	-55		+75	°C
Ilu	Latch up current			+100	mA
Vesd	Electrostatic Discharge – Human Body Model			±2000	V

Stresses at or above those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the following tables is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability (except for the reverse bias condition. See below). Prolonged exposure to high temperatures will shorten the luminance half-life.

Table 5-2 : Recommended Operating Conditions

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD1.8	Front End Power Supply	1.71	1.8	1.89	VDC
VDD5	Array/Analog Power Supply	4.75	5	5.25	VDC
VCOM	Common electrode bias	-5	-2.0	0	VDC
VPG	Array Bias Supply	-3	-1.5	0	VDC
Tst	Storage Temperature	-55		+90	°C
Ta	Ambient Operating Temp.	-45	+25	+70	°C

Table 5-3 : DC Characteristics

(Ta = 25°C, VDD1.8 =+1.8V, VDD5 = +5V, GND = 0V, 60Hz refresh rate)

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD1.8	Front End Power Supply		1.8		V
VDD5	Array/Analog Power Supply		5		V
VCOM	Common electrode bias	-5	-2.0	0	V
VPG	Array Bias Supply		-1.5		V
Vil	Digital input low level	GND-0.3		0.6	V
Vih(1)	Digital input high level	1.2		VDD1.8+0.3	V
Vol	Digital output low level		GND	0.5	V
Voh(1)	Digital output high level	VDD1.8-0.2	VDD		V
VGN	Gamma feedback signal	0		5	V

(1) Except for the SCL and SDA pins for which the high level is in between +1.8 VDC and +5 VDC

Table 5-4 : AC Characteristics

2048 x 2048 format
(-45°C < Ta < +70°C, GND = 0V, VDD1.8= +1.8V, VDD5 = +5.0V,VPG = -1.5V)

Symbol	Parameter	Min	Typ.	Max.	Unit
SCLK	24RGB Source Video Clock Frequency	44	-	580	MHz
CLK_Duty	SCLK duty cycle	45		55	%
Fhs	Horizontal Sync frequency	60		300	KHz
Fvs	Vertical Sync Frequency	50		120	Hz
Trst	Reset Pulse Width	100		-	µs
Cin	Digital Pins Input Capacitance		3		pF
Cvpg	Pin VPG Input Capacitance		13.6		nF
Pd VDD5	Average VDD5 Power Consumption (2K x 2K Mode 60 Hz refresh rate)		600		mW
Pd VDD1.8	Average VDD1.8 Power Consumption (Full screen mode 60 Hz refresh rate)		70		mW
Pd VPG	Average VPG Power Consumption			1	mW
Pd PDWN	Total Power Consumption in PDWN (sleep) mode*		5		mW
Ta	Ambient Operating Temperature	-45		+70	°C

Power consumption measured at 60Hz refresh rate, room ambient temperature and with a TV-like color test pattern that represents an average video mode (See below Figure 2)

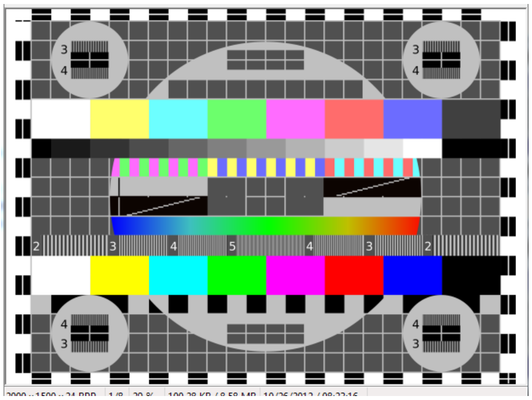


Figure 2: Color Test Pattern

5.1 Timing Characteristics

The timing information provided below relates to the frame and line timing, not the LVDS physical interface (described in section 9.1.1.2 below))

5.1.1 24RGB Source Video Input Timing Requirements

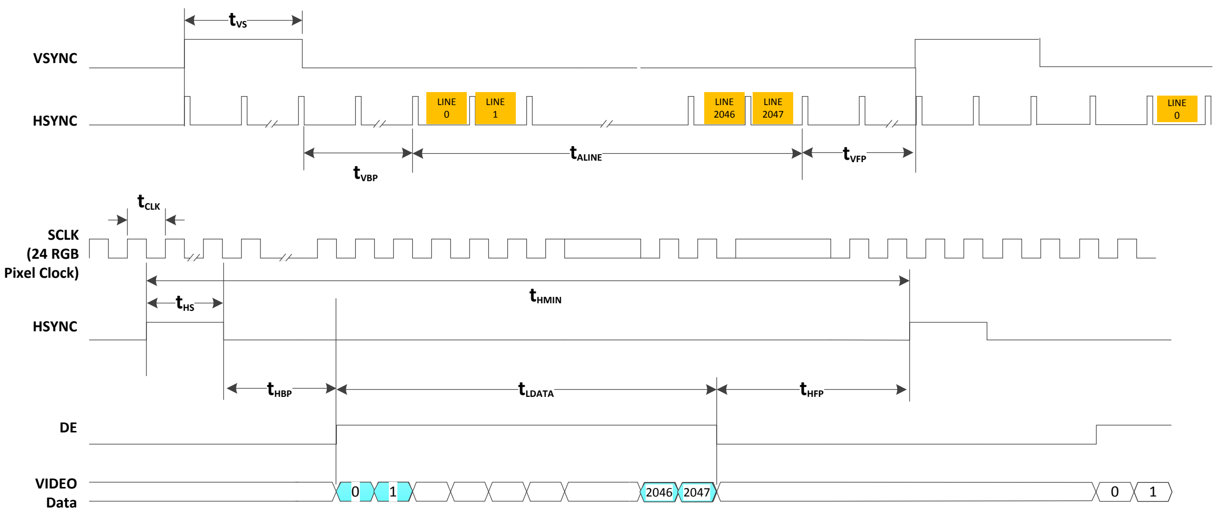


Figure 3: Source Video Timing Requirement

Table 5-5 : Video Input Timing Characteristics (2K x 2K format)

Parameter	**Symbol**	**Min.**	**Typ.**[1]	**Max.**	**Unit**
Clock Frequency Clock Period	SCLK		279		MHz
	t_{CLK}		3.58		ns
Clock Duty	D_{CLK}	45	50	55	%
VSYNC Pulse Width	t_{VS}	3	3		Hsync
V Back Porch	t_{VBP}	3	46		Hsync
V Front Porch	t_{VFP}	3	10		Hsync
Active Video Lines	t_{ALINE}	512	2048	2072	Hsync
HSYNC Pulse Width	t_{HS}	16	32	t_{DES} -8	SCLK
H Back Porch	t_{HBP}	20	80		SCLK
H Front Porch	t_{HFP}	16	48		SCLK
Active Video Pixel	t_{LDATA}	512	2048	2072	SCLK
Minimum H Period	t_{HMIN}	1100 * t_{CLK} + 0.8 us			us

Note 1: 2Kx2K @ 60 0Hz frame rate, Reduced Blanking Mode

5.1.2 Video Formats and Timing

	Video Source									
	Video	Horizontal (Pixels)		Vertical (Lines)		Video Timing				
	Format	No.of Active Pixels/Line	Horizontal Blanking	No. of Active Lines/Frame	Vertical Blanking	Frame Rate	24 RGB Video Clock (Pixel CLK) (MHz)		Horizontal Freq	
		Pixels	Design Requirements	Lines	Design (Minimum)	Hz	Reduced Blanking	VESA	KHz	us
QUAD (18 CH)	2K2K	2048	52	2048	9	138	596.12	666.25	283.87	3.52
	WUXGA	1920	52	1200	9	250	596.04	705.00	302.25	3.31
	1.8K1.8K	1800	144	1800	9	170	597.84	650.50	307.53	3.25
	1.7K1.7K	1700	248	1700	9	180	599.24	619.25	307.62	3.25
	1.6K1.6K	1600	340	1600	9	190	593.08	586.50	305.71	3.27
	UXGA	1600	344	1200	9	250	587.57	610.25	302.25	3.31
	SXGA	1280	664	1024	9	295	592.40	503.25	304.74	3.28
	1k1K	1024	920	1024	9	295	592.40	413.75	304.74	3.28
	512x512	512	1436	512	9	590	598.80	278.50	307.39	3.25
	SVGA	800	1140	600	9	500	590.73	374.25	304.50	3.28
DUAL (10 CH)	2K2K	2048	26	2048	9	70	298.64	327.00	143.99	6.94
	WUXGA	1920	26	1200	9	125	294.09	331.00	151.13	6.62
	1.8K1.8K	1800	26	1800	9	90	297.29	331.25	162.81	6.14
	1.7K1.7K	1700	26	1700	9	100	294.97	330.50	170.90	5.85
	1.6K1.6K	1600	26	1600	9	110	287.79	326.25	176.99	5.65
	UXGA	1600	26	1200	9	150	294.88	340.25	181.35	5.51
	SXGA	1280	26	1024	9	220	296.80	361.00	227.26	4.40
	1k1K	1024	26	1024	9	275	298.28	381.75	284.08	3.52
	512x512	512	456	512	9	580	292.51	272.25	302.18	3.31
	SVGA	800	170	600	9	500	295.37	374.25	304.50	3.28
SINGLE (6 CH)	2K2K	2048	26	2048	9	35	149.32	160.75	72.00	13.89
	WUXGA	1920	26	1200	9	60	141.16	154.00	72.54	13.79
	1.8K1.8K	1800	26	1800	9	45	148.65	162.00	81.41	12.28
	1.7K1.7K	1700	26	1700	9	50	147.49	161.50	85.45	11.70
	1.6K1.6K	1600	26	1600	9	55	143.89	158.75	88.50	11.30
	UXGA	1600	26	1200	9	75	147.44	164.00	90.68	11.03
	SXGA	1280	26	1024	9	110	148.40	170.75	113.63	8.80
	1k1K	1024	26	1024	9	135	146.43	174.50	139.46	7.17
	512x512	512	26	512	9	530	148.56	241.25	276.13	3.62
	SVGA	800	26	600	9	295	148.40	196.75	179.66	5.57

5.1.3 Gamma Sensor Timing Diagram

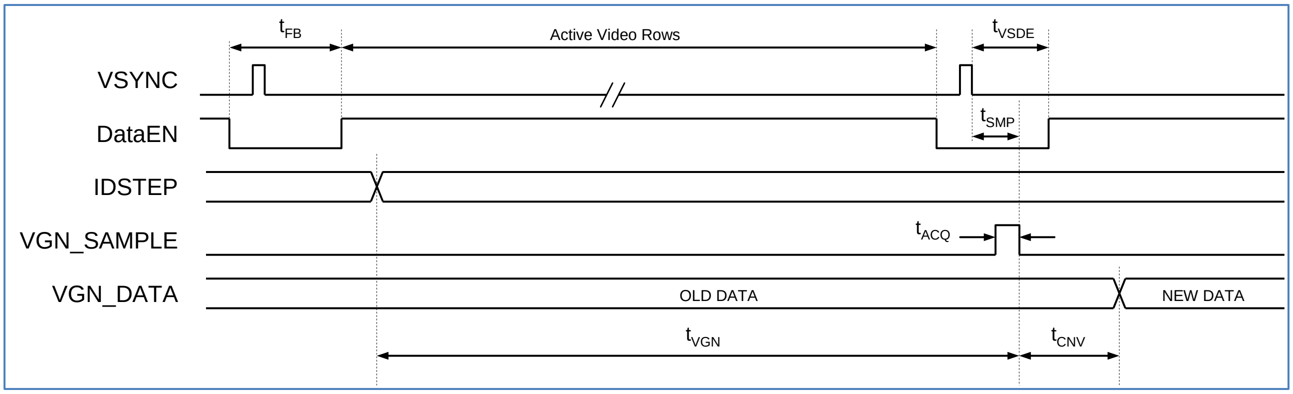


Figure 4: Gamma Sensor Timing Diagram

Table 5-6 : Gamma Sensor Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
IDSTEP to VGN Settling Time	t_{VGN}	10			ms
Frame Blanking (% of Frame Time)	t_{FB}	7			HSYNC
VGN Sampling Time	t_{SMP}	t_{ACQ}		t_{VSDE}	
A/D Acquisition Time	t_{ACQ}	20			μs
A/D Conversion Time	t_{CNV}				

6. OPTICAL CHARACTERISTICS

Table 6-1 : 2K_CFXL Microdisplay Optical Characteristics

Conditions: Ta = +20ºC, VDD1.8 = +1.8V, VDD5 = +5V, VPG = -1.5V, VCOM = internally generated

Symbol	Parameter	Min.	Typ.	Max.	Unit
LMAX	Front Luminance @ max gray level[1]	0.1	150	250	cd/m^2
	Variability (over time)	0	10	22	%
CR	White to Black Contrast Ratio	1,000:1			
CIE	CIE-X	0.270	0.310	0.370	
	CIE-Y	0.320	0.350	0.380	
GL	Gray Levels	-		256	levels
F_R	Refresh Rate	30		120	Hz
FF	Emissive Area/Total Sub-pixel Area		0.75		
U_{LA}	End to end large-area uniformity	85[2]			%
S_{VH}	Pixel spatial noise at ½ luminance (1STD)			5	%
S_{LOT}	Peak-to-peak luminance variation over operating temperature range			8	%
T_{ON}	Time to recognizable image after application of power			0.5	sec

Note 1: At the center of a 100% of gray level box, that does not exceed 60% of the total display area

Note 2: At 100% of gray level brightness and 150 cd/m2 luminance. Luminance uniformity measured between the nominal values of five 1000-pixel zones located in the four extreme corners and the center zone of the display.

7. MECHANICAL CHARACTERISTICS

<u>Connector J1</u>	
Manufacturer:	Hirose
Manufacturer Part Number:	DF12D(3.0)-36DP-0.5V(81)
Mating Connector Information	
Manufacturer:	Hirose
Manufacturer Part Number:	DF12A(3.0)-36DS-0.5V(81)
<u>Connector J2</u>	
Manufacturer:	Hirose
Manufacturer Part Number:	DF12D(3.0)-40DP-0.5V(81)
Mating Connector Information	
Manufacturer:	Hirose
Manufacturer Part Number:	DF12A(3.0)-40DS-0.5V(81)
Weight:	< 5 grams
Printed Circuit Board Material:	FR4
Printed Circuit Board Tolerances:	± 0.2 mm (both axes)

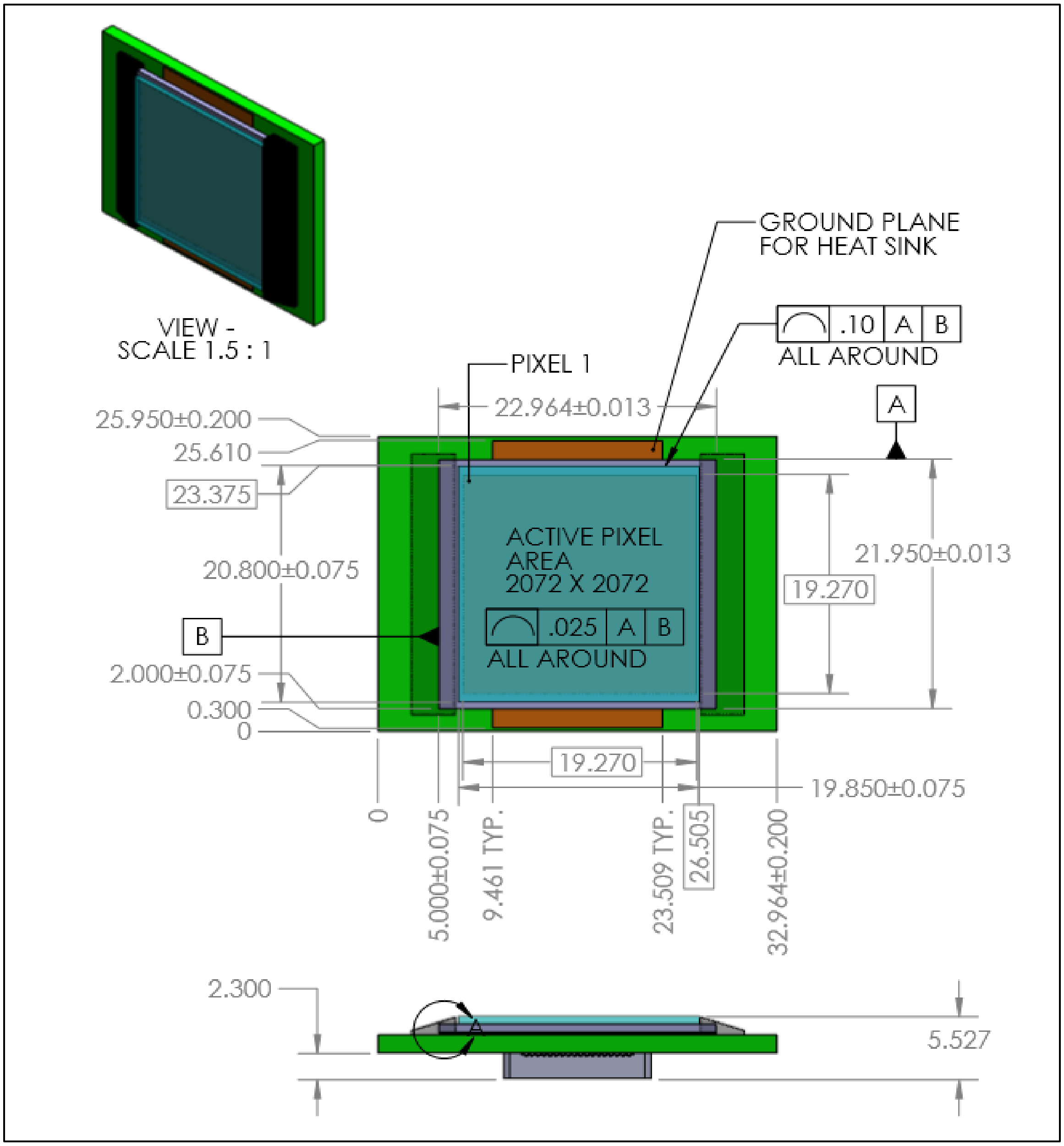
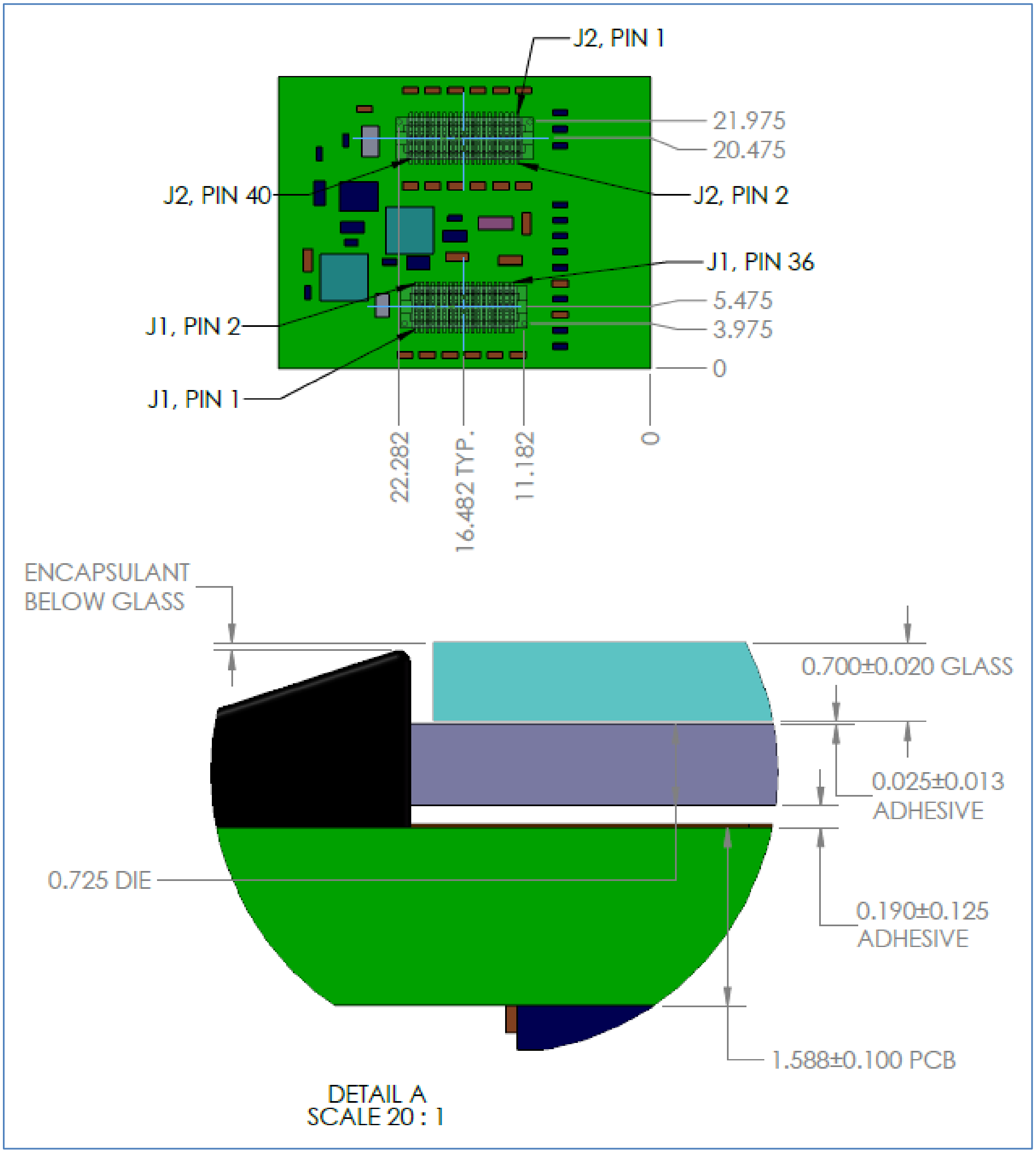


Figure 5: Display-side view of 2K_CFXL microdisplay


J2, PIN 1
21.975
20.475
J2, PIN 40
J2, PIN 2
J1, PIN 36
5.475
3.975
0
J1, PIN 2
J1, PIN 1
22.282
16.482 TYP.
11.182
0
ENCAPSULANT
BELOW GLASS
0.700±0.020 GLASS
0.025±0.013
ADHESIVE
0.725 DIE
0.190±0.125
ADHESIVE
1.588±0.100 PCB
DETAIL A
SCALE 20 : 1

8. CARRIER BOARD SCHEMATIC

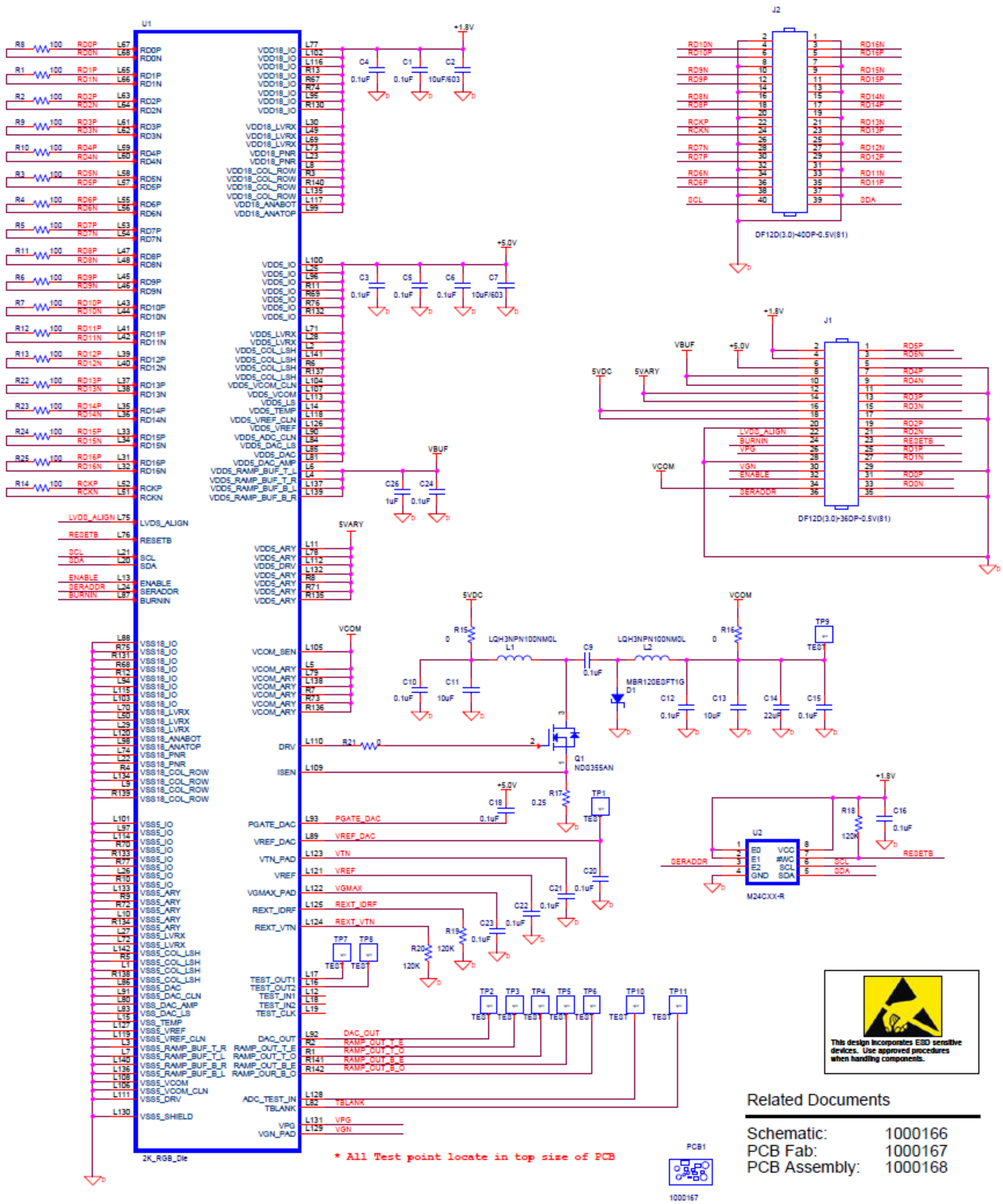


Figure 6: 2K x 2K Microdisplay Carrier Board Schematic

9. DETAILED FUNCTIONAL DESCRIPTION

9.1 Data Interface

9.1.1 Data Receiver

9.1.1.1 Data Alignment

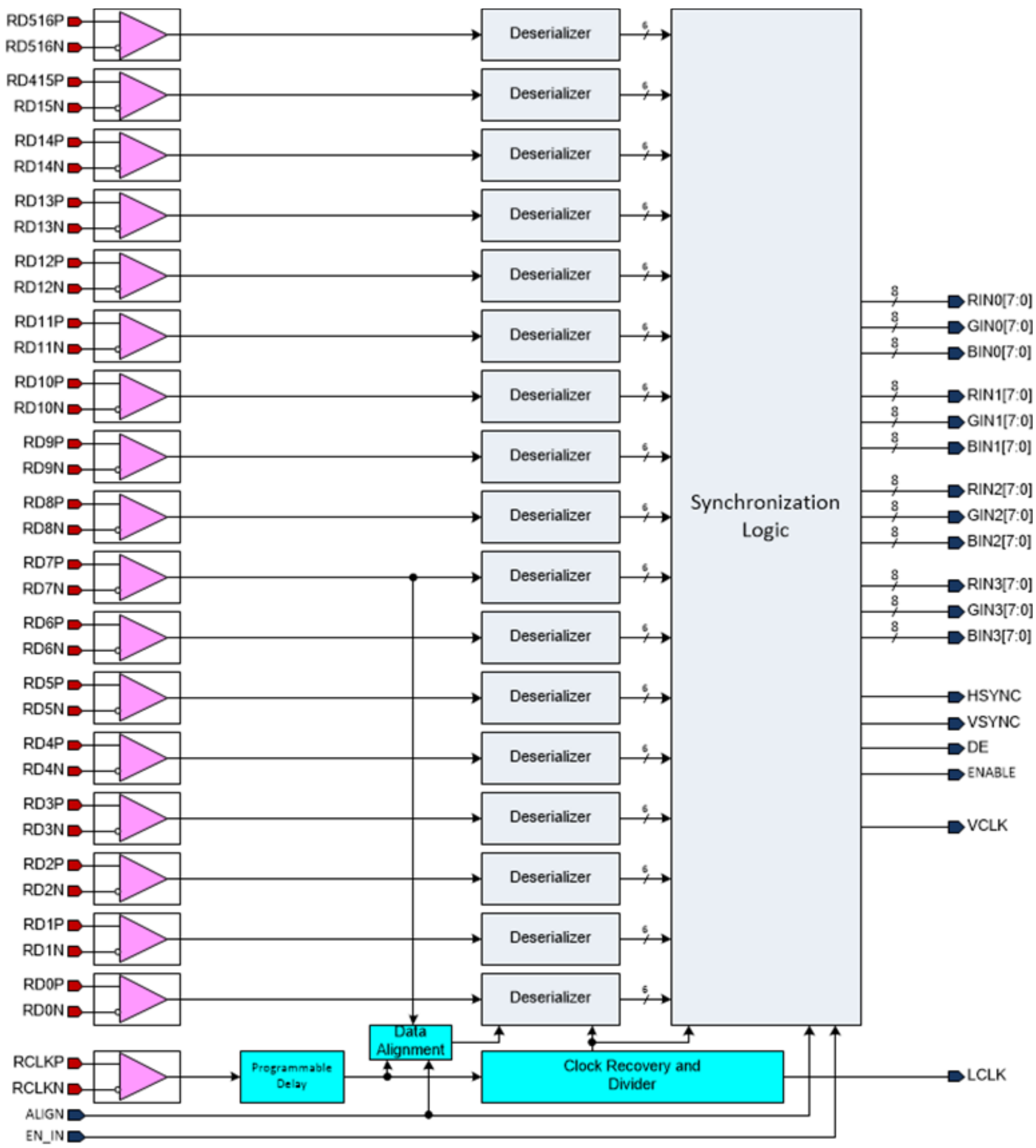


Figure 7: LVDS Receiver Block Diagram

The video interface signals are composed of 17 data pairs and one clock pair, which are the low voltage differential signaling (LVDS), and one control signal(ALIGN), which is a CMOS signal. It is different from the industry standard LVDS interface protocols. The receiver input PADs expect the standard LVDS output signaling levels, but the serialization and protocol is different.

The LVDS data pairs should be 6-bit serialized data. The LVDS clock also should be the serialized signal in the same way to the data channel with toggle pattern instead of PLL clock. It always becomes ¾ times of the 24-bit RGB pixel clock of the source video in case of quad pixel transfer. The LVDS receiver uses both edges of clock. The LVDS receiver expects the alignment patterns via the 8th data channel (RD7) to identify the MSB of the 6-bits serial data at every VSYNC at least.

9.1.1.2 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CM}	Common Mode Input Range		1.0		1.6	V
V_{TH}	Input Differential Voltage Threshold	|Vp-Vn|	400			mV
I_{IN}	Input Current	V_{IN} = 1.8V			±10	µA
		V_{IN} = 1.0V			±10	µA
F_{TCLK}	LVDS Clock Frequency	2k2K@60Hz		209.25	435	MHz
TT_{TCLK}	LVDS Clock Transition Time	F = 400MHz			0.68	ns
DC_{TCLK}	LVDS Clock Duty Cycle	F = 400MHz	45		55	%
SKWMG	Receiver Skew Margin with Deskew	F = 400MHz	200			ps

Table 10-1: LVDS Characteristics

Appendix B (Section 14) provides guidelines to setup the LVDS source side (transmitter) function.

9.2 Format and Timing Control

Various control signals for the horizontal and vertical sequencers that are needed to implement the specified video formats are generated in the Timing & Control Logic block. Registers VINMODE, DISPMODE, LFTPOS, RGTPOS, TOPPOS and BOTPOS using the serial interface set the specific timing parameters.

The display starts up with the array in the off state (black) by default and requires a command to the DISPOFF register bit via the serial interface to turn the display on. This provides the user with an opportunity to change the default startup conditions before a video image is displayed.

Bi-directional scanning is supported in both orientations via the DISPMODE register. Bit VSCAN sets the vertical scan direction, and bit HSCAN sets the horizontal scan direction.

9.2.1 Input Data Configurations

The 2K x 2K microdisplay can be operated in one of three data input mode:

- Quad Pixel Mode
- Dual Pixel Mode
- Single Pixel Mode

Mode selection depends on the active window size and desired refresh rate. Using either Dual or Single pixel modes reduces the number of required LVDS input pairs, which will reduce power consumption as well as interconnect density. The selection is implemented via the two lower bits of register VINMODE and is summarized in Figure 8, which also includes LVDS data mapping.

Dual Pixel Mode(VINMODE =01)

Single Pixel Mode (VINMODE =1X)

LVDS Port	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD16	RIN3[7]	RIN3[6]	RIN3[5]	RIN3[4]	RIN3[3]	RIN3[2]
RD15	RIN3[1]	RIN3[0]	GIN3[7]	GIN3[6]	GIN3[5]	GIN3[4]
RD14	GIN3[3]	GIN3[2]	GIN3[1]	GIN3[0]	BIN3[7]	BIN3[6]
RD13	BIN3[5]	BIN3[4]	BIN3[3]	BIN3[2]	BIN3[1]	BIN3[0]
RD12	RIN1[7]	RIN1[6]	RIN1[5]	RIN1[4]	RIN1[3]	RIN1[2]
RD11	RIN1[1]	RIN1[0]	GIN1[7]	GIN1[6]	GIN1[5]	GIN1[4]
RD10	GIN1[3]	GIN1[2]	GIN1[1]	GIN1[0]	BIN1[7]	BIN1[6]
RD9	BIN1[5]	BIN1[4]	BIN1[3]	BIN1[2]	BIN1[1]	BIN1[0]
RD8	VSYNC		HSYNC		DATAEN	
RD7	RIN0[7]	RIN0[6]	RIN0[5]	RIN0[4]	RIN0[3]	RIN0[2]
RD6	RIN0[1]	RIN0[0]	GIN0[7]	GIN0[6]	GIN0[5]	GIN0[4]
RD5	GIN0[3]	GIN0[2]	GIN0[1]	GIN0[0]	BIN0[7]	BIN0[6]
RD4	BIN0[5]	BIN0[4]	BIN0[3]	BIN0[2]	BIN0[1]	BIN0[0]
RD3	RIN2[7]	RIN2[6]	RIN2[5]	RIN2[4]	RIN2[3]	RIN2[2]
RD2	RIN2[1]	RIN2[0]	GIN2[7]	GIN2[6]	GIN2[5]	GIN2[4]
RD1	GIN2[3]	GIN2[2]	GIN2[1]	GIN2[0]	BIN2[7]	BIN2[6]
RD0	BIN2[5]	BIN2[4]	BIN2[3]	BIN2[2]	BIN2[1]	BIN2[0]

Figure 8: Pixel Mode Selection & LVDS Channel Mapping

9.2.2 Vertical & Horizontal Position Control

The 2K x 2K microdisplay features a reconfigurable active window mode whose size and location can be programmed using the LFTPOS, RGTPOS, TOPPOS and BOTPOS registers as shown in Figure 9.
The minimum window size is 512 x 512. Any attempt to program the registers to yield a smaller window will result in a 512 x 512 window.

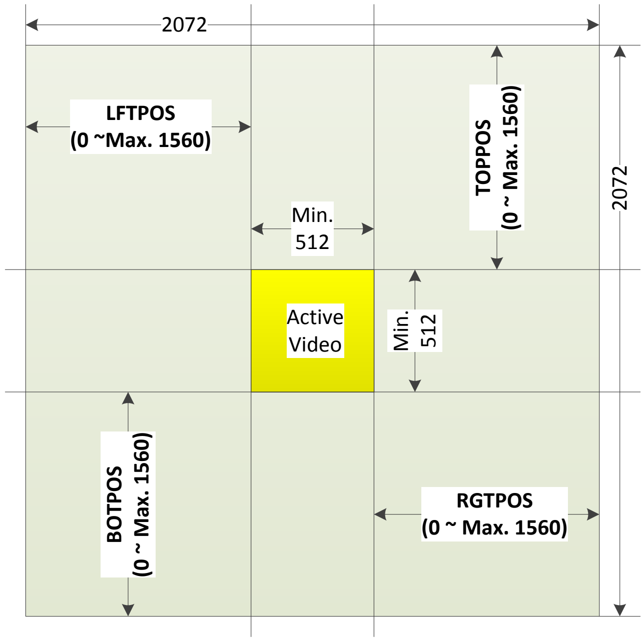


Figure 9 Active Window Configuration

Any part of the display array not covered by the active window size is driven to the black state (no light emission) automatically.
This means that the data source timing can be limited to that required to drive the active window, enabling a lower clock frequency or higher refresh rate for active windows smaller than the full addressable display array (2072 x 2072 pixels).
For example, a 512 x 512 active window can be operated at up to 500 Hz refresh rate, or run at 60Hz with an LVDS clock close to 33 MHz (vs. 210 MHz for 20148 x 2048 active window at 60Hz).
The display power consumption will scale down as the active window size is reduced, assuming a constant refresh rate.

The active window location is defined by the four registers mentioned above (LFTPOS, RGTPOS, TOPPOS and BOTPOS). The location of the active window can be modified on a near real time basis. A 16 ms built-in delay limits the location update to approximately 60 Hz.

9.2.3 Pixel quadrupling

The 2K x 2K microdisplay supports an on-chip pixel quadrupling mode whereby both row and column data are doubled, leading to a maximum supported format of 1036 x 1236 pixels, mapped over the entire 2072 x 2072 addressable pixel area.
This capability allows the use of the full display area as well as an increase of the refresh rate to 240 Hz.
The minimum input format being 512 x 512, the minimum doubled format size is therefore 1024 x 1024 array pixels.

The pixel quadrupling mode is enabled by setting bit 6 (PXLDBL) of register LVDSCTL (03h) to 1

The location of the active window in the pixel quadrupling mode is done via a dedicated set of registers: LFTPOS2, RGTPOS2, TOPPOS2 and BOTPOS2 at addresses 1Ah to 21h

9.3 Gamma Correction

The gamma correction is performed in 8 points piecewise linear interpolator, which convert 8 bit input data to 10-bit gamma compensated data. The linear interpolator requires 8 points LUT coefficients. The gamma LUT coefficients are calculated externally from reading the VGN. In addition, it is possible to use pre-characterized LUT values without calculation.

9.3.1 Manual Gamma

The gamma sensor is provided as an aid to generating a linear optical response from the 2K_CFXL display system. As described previously, an external 8-point set of values are required to transform input video data into a gamma-corrected data signal. The 2K_CFXL display generates an internal real-time representation of the gamma correction curve for the current operating conditions. This representation is in the form of an analog voltage waveform, which can be sampled one point at a time at the VGN pin for eight specific values on the curve. A specific value $\boldsymbol{VGN_i}$, corresponding to one of eight internally fixed grayscale levels $\boldsymbol{GL_i}$, is selected by setting the corresponding IDSTEP bits via the serial port. The VGN signal is internally fixed for a full-scale output range of VDD5/2. Eight sequential measurements are required to complete the pixel response curve. These measurements can then be used to reconstruct an approximation of the ideal gamma correction curve using piece-wise linear interpolation, or by employing a curve fitting algorithm to achieve more accuracy if desired. The outcome of this operation are the 8 points used by the internal interpolator to correct the incoming data according to the desired gamma profile.

An external A/D converter is required to convert each VGN measurement into digitized form and to store the values in a microcontroller for further processing. A full frame period following a change in the IDTEP bit should be provided to allow the VGN signal to settle before sampling it to 10-bit precision by the external A/D converter. It is recommended to sample the VGN signal during the frame blanking interval for best results.

The VGN readings are normalized and converted to a 10-bit full-scale word $\boldsymbol{DVGN_i[9,0]}$ using the following expression:

$$DVGN_i[9,0] = \frac{VGN_i}{VGN_{MAX}} * 1023$$

where ***VGN_{MAX}*** is VDD5/2. Each of these data values must be further multiplied by a correction factor ***CF_i*** to obtain the Gamma table coefficients as follows:

$$GC_i[9,0] = DVGN_i * CF_i$$

where the empirically determined values for factor ***CF_i*** are given in Table 10-3.

Table 10-3: Correction Factor values

CF1	CF2	CF3	CF4	CF5	CF6	CF7	CF8
0.870	0.880	0.900	0.922	0.940	0.955	0.968	1

Using the derived values for ***GC_i*** and their corresponding grayscale coordinates ***GL_i***, the 8-entry Gamma Correction table consisting of data points ***Q_i*** = (***GL_i***, ***GC_i***) can be constructed. The outcome of a typical gamma sensor measurement and calculation procedure is shown in Table 10-4.

Table 10-4: Sample Gamma Correction Table

i	1	2	3	4	5	6	7	8
IDSTEP[0]	0h	1h	2h	3h	4h	5h	6h	7h
VGN_i (volt)	1.839	1.876	1.913	1.964	2.045	2.159	2.318	2.500
GC_i (dec)	331	349	364	383	407	436	471	511
GL_i (dec)	2	4	8	16	32	64	128	255

The 2K x 2K microdisplay uses the GC_i values in the data interpolator function. The interpolator calculates the intermediate points in real time using a linear interpolation between the two anchor points that bracket the incoming 8-bit data.
8 Registers (LUT0 through LUT8) are used to store the GC_i values (10 useable bit each). Although the 2K x 2K CFXL microdisplay uses a white broadband emitter, it is possible to configure a different gamma response for each of the R, G and B data paths. Register UDGAMMA bits [2..0] can be used to select the color channel, and register UDGAMMA bit 3, when set to 1, will update the selected color interpolator with the GC_i values.

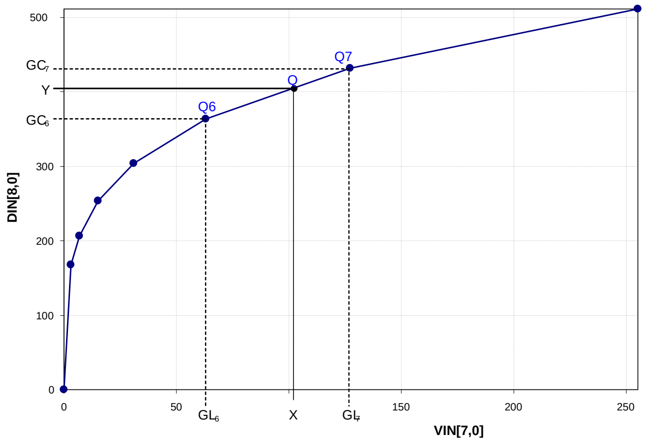


Figure 10 : Generating intermediate points by linear interpolation

A smooth transition of the gamma curve at the lowest gray levels is essential for best performance of the display at the black end of the gray scale. Refer to Figure 11 for an illustration of the recommended approach for calculating the gamma curve at low gray levels. The LUT data points for gray levels 1 to 4 are by linear extrapolation from the gamma points Q1 and Q2. The LUT data point for gray level 0 (also defined as Q0) is a fixed value that is user-defined, and normally should be set to a very low value, e.g. 1, to ensure the best black level. The value for Q0 is shown on the graphical interface screen supplied with the 2K_CFXL design reference kit for user convenience. It is not affected by the gamma sensor signal and can only be changed manually by user input.

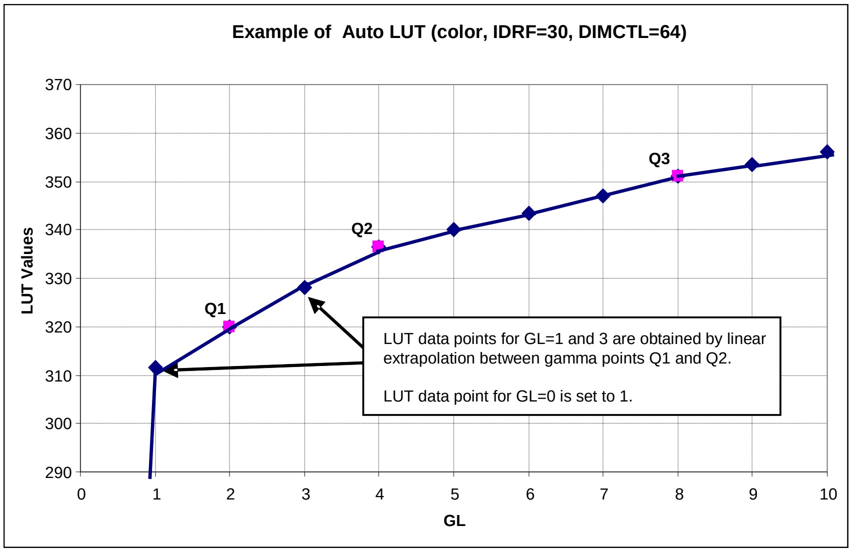


Figure 11 : Gamma curve at low gray levels

An arbitrary optical response function for the microdisplay can be obtained by performing an additional operation on the gamma coefficients before generating the gamma correction curve as described previously. For example, the relationship between the output luminance of the display

(y) and the gray level input to the LUT (x) can be defined in terms of the system gamma (γ) by the following expression:

$$y = x^{\gamma}$$

The corresponding gamma coefficients are then given by the following expression:

$$GC_i^{\gamma} = \left(\frac{VGN_i}{VGN_{MAX}} * CF_i \right)^{\gamma} * 1023$$

For the case of a linear optical response (γ=1) this expression reduces to the simpler form given previously. Examples of gamma curves generated from the same VGN values for different settings of the System Gamma parameter are shown in Figure 12 and the corresponding system response curves for the display are given in Figure 13.

The System Gamma function is implemented in the DRK Firmware and is accessible to the user in the DRK GUI Software (MS Windows 7 & 10 compatible).

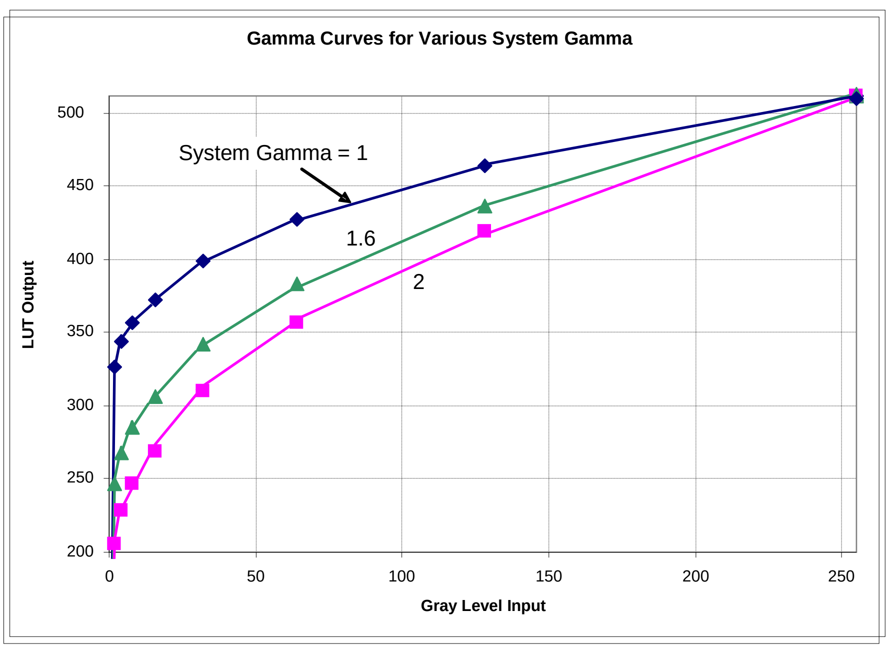


Figure 12 : Gamma curves for arbitrary System Gamma

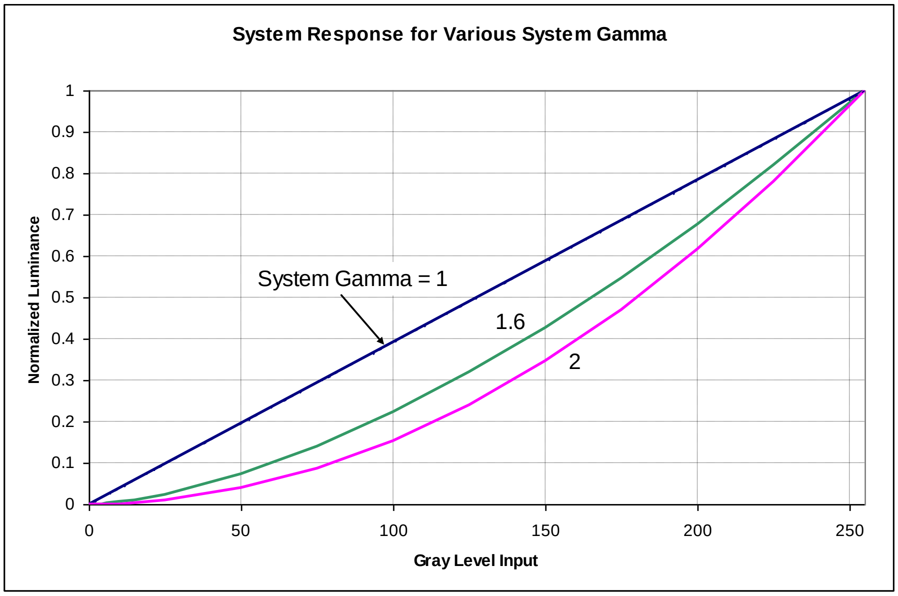


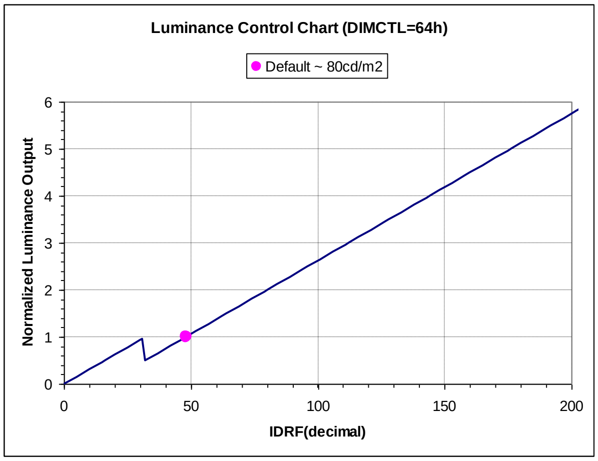
Figure 13 : Display system response for arbitrary system gamma

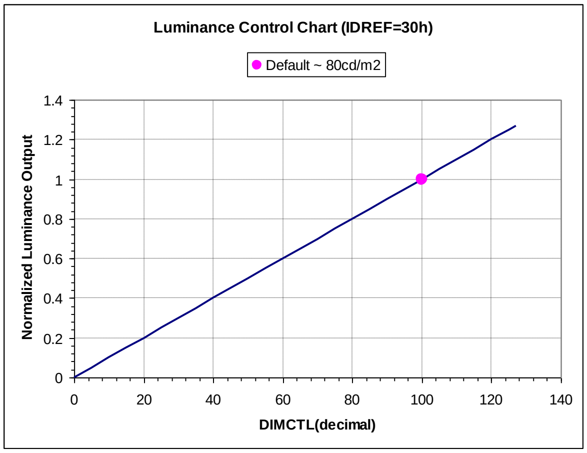
9.4 Brightness Control

9.4.1 Analog Dimming

A variable luminance level is achieved by controlling the maximum pixel current while maintaining the largest possible dynamic range. Dimming control for the display is achieved by adjusting the 7-bit register DIMCTL via the serial interface to provide 128 linear steps in brightness ranging from near zero to the maximum level set by register IDRF. This functionality is only available for VCOMMODE=0 or 1.

The bits IDRF_COARSE in register IDRF provide a coarse adjustment of the maximum luminance level, while the IDRF_FINE bits enable the coarse level to be fine-tuned. Figure 14 shows the typical luminance output at gray level = 255 in a color display for various settings of the IDRF and DIMCTL registers.





(a) (b)

Figure 14: Typical maximum luminance for various IDRF (a) and DIMCTL (b) settings

9.4.2 Pulse Width Modulation Dimming – Rolling Shutter

The duty rate for a row of data is defined as the fraction of a frame period during which the pixels maintain a programmed value; for the remainder of the frame period the pixels will be driven to black.

A Row Reset function is provided in the 2K display to allow the duty rate of rows to be controlled between 0 and 100% (default condition). The register ROWRSET[12,0] is used to set the number of Hsync cycles during which the pixel data is driven to black during a frame period. For ROWRSET=0 the pixel data is never driven to black and the duty rate for pixel data is equal to 100% (default). For ROWRSET=W the pixels in any row are driven to black for the final 2*W Hsync cycles in an active frame period.

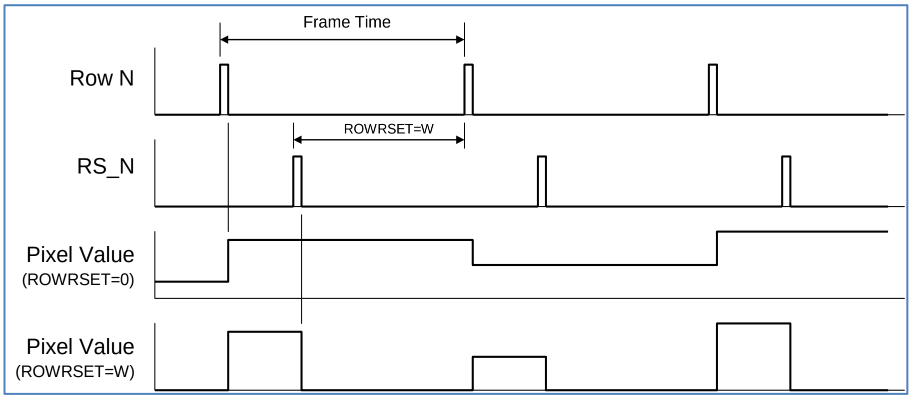


Figure 15 : Timing diagram showing Row Reset functionality.

The operation of the Row Reset function is depicted in the timing diagram shown in Figure 15. All the pixels contained in ROW N are programmed during the Nth horizontal line scan following the initialization line scans, which occur at the beginning of a video frame. Normally this pixel data is stored in the pixel and remains unchanged until it is refreshed during the next frame period. When the Row Reset function is activated, the pulse RS_N is generated at a position determined by the value of register ROWRSET. For example, when the register value is equal to W the rising edge of RS_N occurs exactly 2*W Hsync cycles prior to the next programming cycle for ROW N. The pulse RS_N sets all the pixels in ROW N to black until the next programming cycle. All rows in the array will operate at the same duty rate. As a result, the duty rate for all the rows in the pixel array will be given by

$$ROW\_DUTY = \frac{T_{FRAME} - 2 * W * T_{HSYNC}}{T_{FRAME}}$$

9.5 Global Shutter

The 2K x 2K microdisplay has the ability to be operated in a “global shutter” mode whereby the data is displayed only once all the active rows have written to, and for a defined period of time. The VPG input is used to control the light emission on an array basis. By modulating this input between two voltage levels, and by using a dedicated video timing format that provides time between the last valid data line and the start of the next frame (leading edge of the Vertical Sync signal, typically), an “on-time” period can be defined during which VPG is brought low to is nominal -1.5 Volts level to turn on the entire display at once.

At the time of this datasheet version, there is no established industry standard for Global Shutter modes. It is therefore up to the system integrator to provide the correct timing format in order to leverage this capability.

9.6 Active Matrix Drive

In this design, the conversion of the video input signal into an analog drive signal at the pixel is carried out in a two-step process during each horizontal clock period. The digital input video data is first transformed into a precise time delay based on counts of the global RAMP clock. Second, the time delay triggers the column switch to sample the voltage of a linear ramp and to store the analog value on the column line capacitor. The selected pixel circuit copies the analog data and uses it for driving the OLED diode until it is refreshed during the next frame period.

A block diagram of one column drive circuit is shown in Figure 16. The 2072 Display registers form a line memory that facilitates a pipeline mode of operation in which video data is converted to analog form and sampled by the pixels in row M during the same line period that video data for row M+1 is loading into the Load registers. At the end of each line period, the data in the LOAD registers is transferred in parallel into the Display line memory. The divide-by-4 of SCLK clock is used for both loading input data into the chip and for advancing the global column counter. There is a maximum latency of 2 line periods before data is displayed.

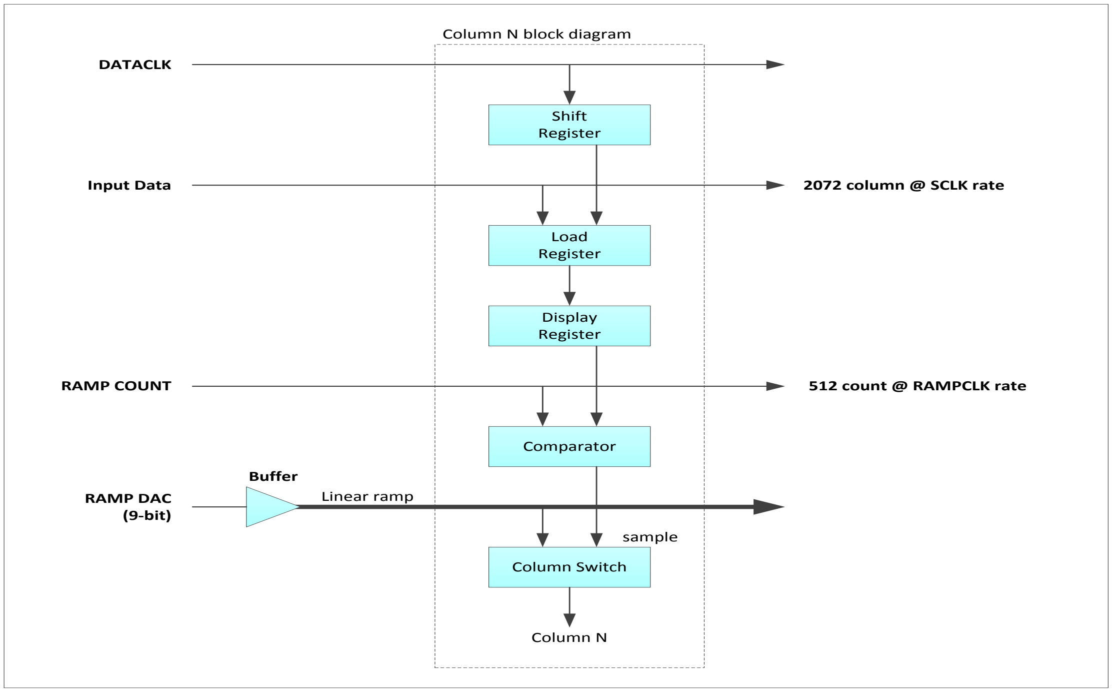


Figure 16: Data sampling for Column N

A timing diagram for the data sampling process is shown in Figure 17. The internal Ramp Generator operates at the HSYNC frequency and outputs a linear ramp with a slow rise-time and a fast reset capability that is buffered and applied to all the pixel array columns simultaneously. The RAMP signal starts synchronously with HSYNC (after a delay) with a positive slope from a zero voltage level and rises to a voltage near the VDD5 rail after 1024 SCLK clock cycles as determined by a 10-bit counter. The start position of the RAMP can be adjusted via register bits RAMPDLY, its peak value can be set using register VDACMX, and the duration of the flyback transition can be selected between two options by the FLYBTIME bit in register RAMPCTL.

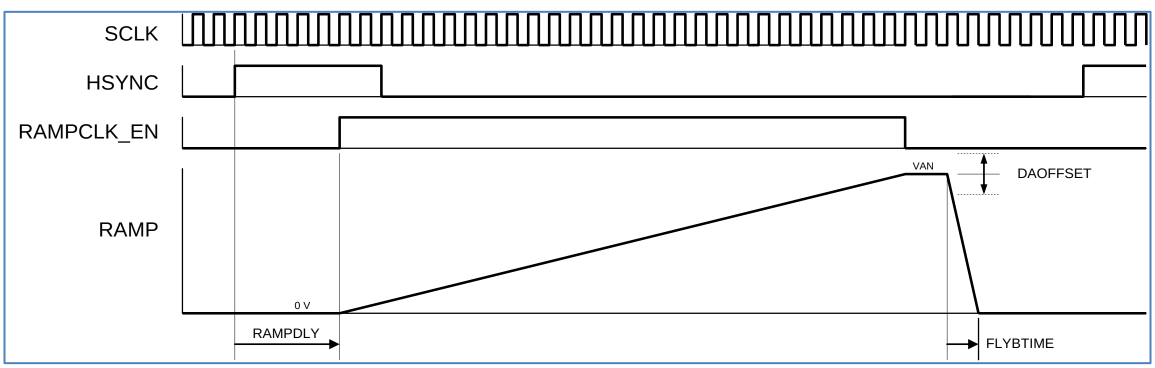


Figure 17: Timing diagram for column data sampling

Register BIASN[2,0] sets a bias current for the OLED array in order to achieve improved control of black level and color saturation at the expense of a small increase in power consumption. It is recommended to use the BIASN=7 setting for best performance.

9.7 On-chip DC-DC Converter

An on-chip dc to dc converter controller allows for the generation of the OLED cathode supply, relying on a few external passive components assembled on the display carrier board. The converter is an adjustable inverter that converts VDD5 to a negative supply used to bias the OLED via the VCOM input pin. Adjustment is managed by the control logic and registers VCOM[7,0], VCOMCTL[7,0] and VCOMMODE[3,0].

The converter adjustment comes from two sources:

- A nominal value set in a dedicated register that provides for the room temperature voltage level.
- The output of an internal VCOM sensor circuit. This feature can be enabled/disabled via register setting to allow full external control (via register VCOM).

A block level schematic of the Cuk converter that is implemented in the 2K_CFXL application is shown in Figure 18.

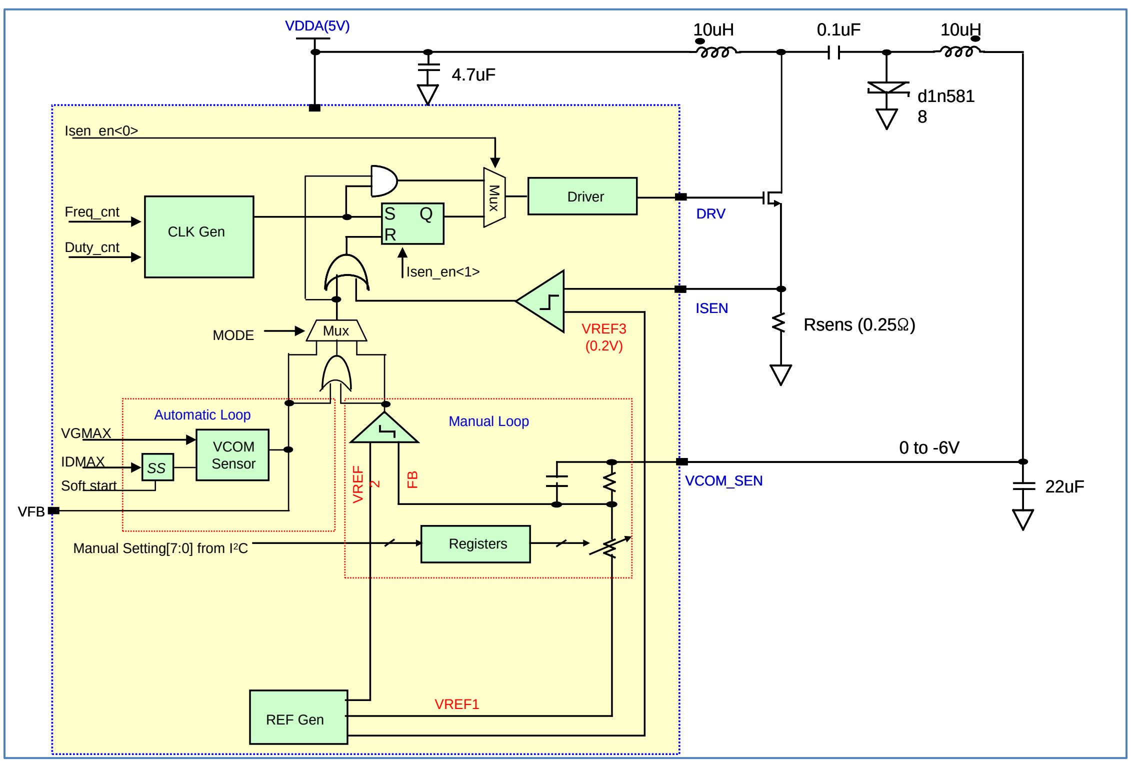


Figure 18 : Schematic of DC-DC controller function

Mode 1, selected by default (VCOMMODE=0), activates the Automatic Loop which provides VCOM regulation based on an internal current feedback sensor. In this mode, the cathode supply is automatically regulated in order to maintain a constant maximum OLED array current over changes in temperature and luminance. The cathode voltage will tend to rise in absolute value as the luminance level is increased or the operating temperature is reduced.

9.8 Temperature Sensor

An on-chip temperature sensor provides continuous device temperature information via the serial interface. The sensing circuitry allows for calibration at power-up via dedicated registers, TREFDIV[5,0] and TEMPOFF[7,0]. The temperature reading is digitized on-chip and stored in a dedicated register, TEMPOUT[7,0]. A register bit, TSENPD in register ANGPWRDN, is able to power down the sensor.

The temperature sampling period is controlled by register TUPDATE[7,0] which allows the temperature reading to be updated between every 50msec to 4.25sec when operating at a 60Hz frame rate.

9.8.1 Luminance Regulation Sensor

Register VGMAX[7,0] controls the pixel drive voltage used for regulating the maximum luminance value. By default this level is set to about 4.95V when the VDD5 supply is equal to 5V to avoid saturating the video buffers. It can be adjusted over a range of 4 to 5V.

Register VDACMX[7,0] is used to set the maximum value of the internal Ramp DAC generator. This value should match the internal VGMAX setting for best luminance accuracy and control. The optimum setting has been determined by measurements to be 7A for normal operating conditions. Refer to section 11.11 for more detail.

9.9 Power Consumption Management

9.9.1 Power Sequencing

To ensure proper startup and stabilization of the display the following power-on sequence is recommended:

1. Turn on VDD1.8, VDD5 and VPG supplies (these can be simultaneous)
2. Wait about 1ms before releasing the RESETB signal
3. Configure the display registers to the desired startup state
4. Turn on the display by setting the DISPOFF bit in register DISPMODE to “0”

Figure 19 shows the timing diagram for the power supplies and control signals during startup when the display is first turned on. The external supply voltages (VDD5, VDD1.8, and VPG) can all be applied at the same time as in the diagram. An internal power-on-reset signal is triggered when both the VDD5 and VDD1.8 voltages exceed a built-in threshold level. After a delay of about 70ms the internal dc-dc controller is activated which generates a negative supply for the common cathode of the array. The video display is enabled 20ms later and video is displayed on the array after the DISPOFF bit has been set to “0” via the serial port. Prior to this moment, the pixels in the array are actively driven to the black state. The pin RESETB must also be logic high before any registers can be written.

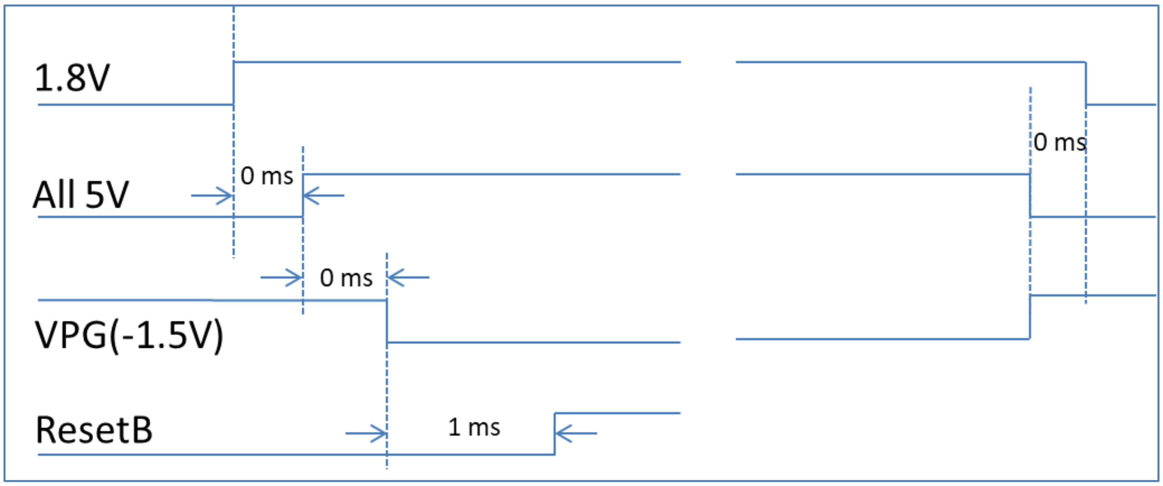


Figure 19: Power-Up/Down Sequence

9.9.2 Display Off Function

On power-up the microdisplay sets all internal registers to their default values and holds the array in the black state until a display off register is externally enabled. The DISPOFF bit in the DISPMODE register must be set to zero via the serial port in order for the array to become active.

9.9.3 Power Saving Modes

The circuit provides power down modes to minimize power consumption. This can occur in two ways:

- Sleep mode – manually controlled via the PDWN bit in register SYSPWRDN, the entire display chip is powered down except for the serial interface. The register settings are saved and restored on power up from this mode.
- Individual block control - many functional blocks have the option to be turned off individually via control of registers ANGPWRDN and SYSPWRDN.

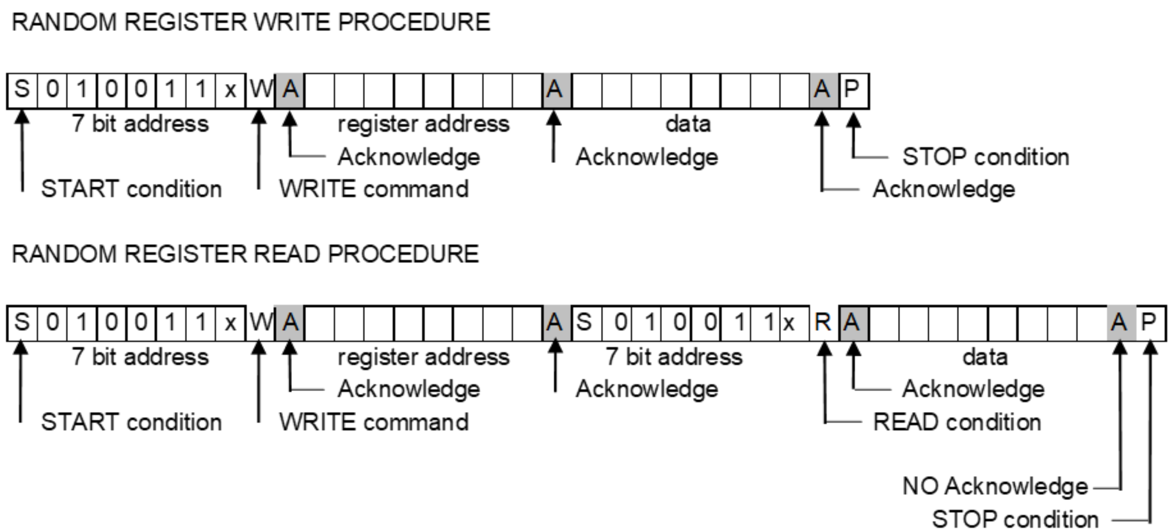
9.10 Serial Interface

The serial interface consists of a serial controller and registers. The serial controller follows the I2C protocol. An internal address decoder transfers the content of the data into appropriate registers. The protocol will follow the address byte followed by register address data byte and register data byte sequence (3 bytes for each register access):

Serial address with write command
Register address
Register data

The registers are designed to be read/write. Read mode is accomplished via a 4-byte sequence:

Serial address with write command
Register address
Serial address with read command
Register data



The serial controller is capable of slave mode only.

The x in the 7-bit address code is set by the SERADD input pin and is provided to allow a dual display and single controller configuration.

Slave Address: 010011X where X = 0 or 1 depending on the status of the SERADD pin.

Write Mode: Address is 4C (or 4E if SERADD = 1)

Read Mode: Address is 4D (or 4F is SERADD =1)

Sequential Read/Write Operation

The serial controller allows for both sequential and read operational modes. For either mode, the host needs only set the initial register address followed by as many data bytes as needed, taking care not to issue a STOP condition until all desired data bytes have been transmitted (or received).

It is possible to run the I^2C interface without source clock or any sync signals.

Interface maximum frequency: 400 KHz.

9.11 Personalization EEPROM

Each 2K x 2K micro display contains an EEPROM memory device to serve as non-volatile data storage for retrieving display specific information, such as its serial number and optimal registers values for proper operation. The data can be accessed via the same I^2C serial interface that is used to communicate with the micro display. The EEPROM'S serial address is as follows:

SERADDR = 0

Write Mode: Address is A6h

Read Mode: Address is A7h

SERADDR = 1

Write Mode: Address is AEh

Read Mode: Address is AFh

The first 15 bytes represent the serial number of the micro display. The following 68 bytes contain sequential data values that can be used to write to the micro display's internal registers starting with eeprom address 16 to 84.

Addresses 00 to 0Fh should not be changed as they contain serial number and traceability information

Address 10h corresponds to register 00h, which is a read-only register in the microdisplay.

Addresses 11h to 85h correspond to registers 01h to 76h in the microdisplay

Addresses 1Dh, 26h, 27h, 76h, 77h, BCh, BDh, BEh and BFh contain calibrated values specific to each display and should not be changed

Address 1Dh contains the IDRF value needed to reach 150 cd/m^2 at room ambient
Addresses 76h and 77h contain the on-chip temperature sensor calibration values, needed to correctly measure the display temperature
Addresses BCh-BFh contain the information needed to calculate the IDRF needed set an absolute luminance (in cd/m^2).

Addresses 98h to B7h contain the VGN data measured during production testing for the value of IDRF that results in a 150 cd/m2 all pixels on luminance (VGNA series, 8 data 10-bit data values), and IDRF = 20h (lower luminance). These values are provided for reference only and are not needed for normal microdisplay operation.

Registers defined as RESERVED should not be changed.Addresses beyond BFh are blank and may be used.

NOTE1: The EEPROM is not write-protected and care should be taken not to activate the Write Mode. The values highlighted in gray are measured at the factory and are specific to each individual device.

NOTE2: For the current revision of the microdisplay (rev A), the EEPROM is not programmed and all locations will return 0xFF. eMagin Corporation will publish a datasheet release when this situation has been resolved

9.12 Pattern Generator

The microdisplay includes a built-in test pattern generator to simplify the external hardware requirements for test of OLED microdisplays and applications. A dedicated input (BURNIN, J1-24) can be used to automatically set the microdisplay to use the internal pattern generator without need for external data or control signal (the LVDS inputs do not need to be connected). The display starts in this mode with a simple, flat white field at maximum luminance by default and without the need for register setting.
The Test Pattern Generator can also be is activated by setting bit 3 (PATTEN) of register 14h (TPMODE) to 1.

When using the internal pattern generator, it is still possible to control the micro display luminance, but this requires the use of dedicated registers:

Use register 2Bh (IDRF_BN) in lieu of register 0Eh (IDRF)
Use register 2Ch (DIMCTL_BN) in lieu of register 0Fh (DIMCTL)

By default, an all-pixels-on pattern will be displayed. Line test patterns where the line width and space (row and/or column) can be configured through additional registers.
The pattern generator operates independently of the LVDS interface and therefore can be used to troubleshoot system integration issues, as well as during system level testing.
The frame rate of the pattern generator can also be adjusted from 30Hz to 120Hz (four options) using the FRSEL bits (bits 5-4) of the TPMODE register.

Please refer to the detailed TPMODE register description (section 11.16) for information on how to setup and use the internal pattern generator

Figure 20 illustrates the application setup for the chip in BI mode using the built-in test functionality.

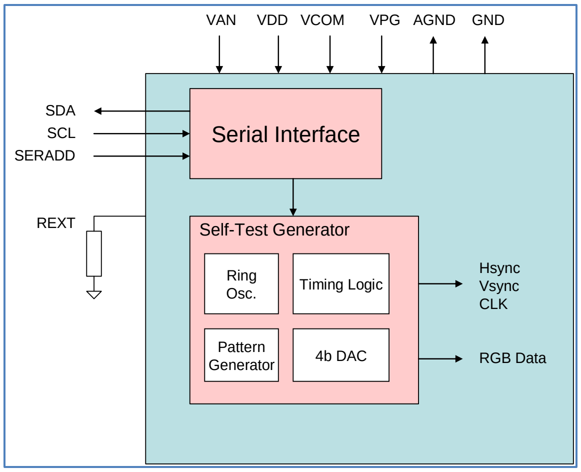


Figure 20 : Block diagram of setup for BI mode

10. REGISTER MAP SUMMARY

Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description
00	STAT	R	REV	2-0	0	Silicon Revision Number
01	VINMODE	R/W	WRDISABLE	7	0	I^2C Register Write Disable 0 = Write Enable, 1 = Write Protected (Read Only)
			-	6-3	0	Blank - Not used
			SET_ENABLE	2	0	ENABLE Active Level 0 = ENABLE active low, 1 = ENABLE active high
			VSYNCPOL	1	1	VSYNC Polarity 0 = Negative Sync, 1 = Positive Sync
			HSYNCPOL	0	1	HSYNC Polarity 0 = Negative Sync, 1 = Positive Sync
02	DISPMODE	R/W	DISPOFF	7	1	Display Off 0 = Display On, 1 = Display Off
			POS2EN	6	0	Select Window position registers for Pixel Doubling mode (PXLDBL=1) 0 = Use LFTPOS ~ BOTPOS registers, 1 = Use LFTPOS2 ~ BOTPOS2 registers
			MONO	5	0	Mono Video Input/Display Mode 0 = Color Video Input, 1 = Mono Video Input
			RESERVED	4	0	Do not change this bit (keep it set to 0)
			RESERVED	3-2	0	Do not change these bits (keep them set to 0)
			VSCAN	1	0	Vertical Scan Direction 0 = Top to Bottom Scan, 1 = Bottom to Top Scan
			HSCAN	0	0	Horizontal Scan Direction 0 = Left to Right Scan, 1 = Right to Left Scan
03	LVDSCTL	R/W	PXLDBL	6	0	Pixel Doubling mode Enable 0 = Normal Display mode, 1 = Pixel Doubling mode
			VIDMODE	5-4	0	Video port mode select 00 = Quad Video Input, 01 = Dual Video Input, 10/11 = Single Video Input
			CLKDLY	3-0	0	Select clock delay for serial data latch 0 = no delay, 1 = one unit delay, …. ,15 = 15 unit delay
04	LFTPOS	R/W		7-0	00C	Column Display Left Position
05				10-8		
06	RGTPOS	R/W		7-0	00C	Column Display Right Position
07				10-8		
08	TOPPOS	R/W		7-0	00C	Row Display Top Position
09				10-8		
0A	BOTPOS	R/W		7-0	00C	Row Display Bottom Position
0B				10-8		
0C	ROWRESET	R/W		7-0	0	Row Duty Control
0D				10-8		0:Disable, Each line displayed ROWRESET*2 Line period
				12	0	ROWRESET work on UNENABLED frame in 3D mode
0E	IDRF	R/W	IDRF_COARSE	7-5	0	Coarse adjustment for array reference current
			IDRF_FINE	4-0	0	Fine adjustment for array reference current
0F	DIMCTL	R/W		6-0	01	Dimming level control (default = 1X IDRF)
10	IDSTEP	R/W		2-0	0	Current level for gamma sensor
11	VCOMCTL	R/W	RESERVED	4-2	3	Do not change from the default value (011)
			VCKSEL	1-0	3	Do not change from the default value (011)

Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description
12	TEMPOUT	RO		7-0	-	Temperature Sensor Readout
13	PWRDOWN	R/W	SYSPD	4	0	All System Power Down
			-	3-2	0	Blank
			VCOMPD	1	0	VCOM Power Down
			TSENPD	0	0	Temperature Sensor Power Down
14	TPMODE	R/W	TPVCLK	6	0	Enable External clock for Burn-In-Test-Mode (0 = use internal ring OSC, 1 = use external clock)
			FRSEL	5-4	0	Change speed of internal oscillator (00=60Hz F/R, 01=30Hz, 10=80Hz, 11=120Hz)
			PATTEN	3	0	Test Pattern Display Enable when "1"
			PATTSEL	2-0	0	Select test pattern for Built-In-Test-Mode (BURNIN pin = 'High' or PATTEN = 1) 000= Burn-in (all white), 001=Color Bar, 010=16 level gray scale 011=Checker Board, 100=Vertical Line, 101= Horizontal Line, 110=Grid Pattern
15	RESERVED	R/W		7-0	06	Do not change from the default value (06)
16	RESERVED	R/W		7-0	03	Do not change from the default value (03)
17	VDACMX	R/W		7-0	80	Ramp DAC Max Value Control, -40% ~ +40 %
18	VGMAX	R/W		7-0	0D	Fine adjustment for VGMAX level (default = 4.95V)
19	ADVNCED	R/W		0	0	Advanced control mode Enable (activate more control registers - 60H~88H) 0 = normal user mode, 1 = advanced user mode
1A	LFTPOS2	R/W		7-0	00C	Column Display Left Position for Pixel Doubling windows
1B				10-8		
1C	RGTPOS2	R/W		7-0	00C	Column Display Right Position for Pixel Doubling windows
1D				10-8		
1E	TOPPOS2	R/W		7-0	00C	Row Display Top Position for Pixel Doubling windows
1F				10-8		
20	BOTPOS2	R/W		7-0	00C	Row Display Bottom Position for Pixel Doubling windows
21				10-8		
22-29	-					Blank - Not used
2A	DISPMOD_BN	R/W		7-0	00	DISPMODE register set for Burn-In (automatically replace when Burn-In mode)
2B	IDRF_BN	R/W		7-0	30	IDRF register set for Burn-In (automatically replace when Burn-In mode is selected)
2C	DIMCTL_BN	R/W		6-0	64	DIMCTL register set for Burn-In (automatically replace when Burn-In mode is selected)
2D	GMCTL	WO	CLEAR_FLAG	7	0	VGN _FLAG clear when write "1"
		RO	VGN_FLAG	6-4	0	bit6=ADC STM busy, bit5=VGN7_low, bit4=VGN level higher than upper VGN
		R/W	**SGFSEL**	3-2	0	Select System Gamma Factor 00=Custom SGF (use SGF0~SGF7), 01=SGF-1.2, 10=SGF-1.6, 11=SGF-2.0
		R/W	GAMMASEL	1-0	0	Select Internal Gamma operating mode 00=Manual Gamma mode, 01=Full automatic update, 10=Semi-auto update, 11=Do not use
2E	EVNTMSK	R/W	MSK_IDRF	3	0	Mask IDRF Change event when full automatic update mode (GAMMASEL=01)
			MSK_DIMC	2	0	Mask DIMCTL Change event when full automatic update mode (GAMMASEL=01)
			MSK_VGMAX	1	0	Mask VGMAX Change event when full automatic update mode (GAMMASEL=01)
			MSK_TEMP	0	0	Mask TEMPOUT Change event when full automatic update mode (GAMMASEL=01)
2F	UDGAMMA	WO	GC_UPDATE	3	0	Gamma coefficients update action when write "1" for GAMMASEL = 00, 10 mode
		R/W	GC_RGB	2-0	7	Write selected R,G,B Gamma coefficients (ex. 001=Blue Gamma write enable), applied on all Gamma mode
30	GC0	WO		7-0	007	Coefficient 0 for manual Gamma
31				9-8		
32	GC1	WO		7-0	00F	Coefficient 1 for manual Gamma
33				9-8		
34	GC2	WO		7-0	01F	Coefficient 2 for manual Gamma
35				9-8		
36	GC3	WO		7-0	03F	Coefficient 3 for manual Gamma
37				9-8		
38	GC4	WO		7-0	07F	Coefficient 4 for manual Gamma
39				9-8		
3A	GC5	WO		7-0	0FF	Coefficient 5 for manual Gamma
3B				9-8		
3C	GC6	WO		7-0	1FF	Coefficient 6 for manual Gamma
3D				9-8		
3E	GC7	WO		7-0	3FF	Coefficient 7 for manual Gamma
3F				9-8		

Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description
40-5F	RESERVED	R/W	RESERVED	7-0	0	Do not change
60	RAMPCTL	R/W	RESERVED	7-0	01	Do not change
61	RAMPCM	R/W	RESERVED	7	44	Do not change
62	BIASN	R/W	RESERVED	4	0	Do not change
			RESERVED	3	0	Do not change
			BIASN	2-0	1	000 = bias current off 001~111 = bias current set to 0.5nA, 1nA, 1.5nA, 2nA, 2.5nA, 3nA, 3.5nA
63	VGNSHCTL	R/W	RESERVED	2-1	0	Do not change
			VGNSH_EN	0	0	VGN Sample & Hold Enable 0 = VGN SH Bypass, 1 = Enable VGN SH output
64	VCOMMODE	R/W	RESERVED	7-0	04	Do not change
65	RESERVED	R/W	RESERVED	2	1	Do not change
66	RESERVED	R/W		7-0	51	Do not change
67	TREFDIV	R/W		5-0	2A	Temp. Sensor Reference Clock Divider
68	TEMPOFF	R/W		7-0	87	Temp. Sensor Offset
69	TUPDATE	R/W		7-0	FF	Number of frames per TEMPOUT update (Data range 02H ~ FFH) Update Time = (TUPDATE+1) * $PERIOD_{FRAME}$ $PERIOD_{FRAME}$ = 16.6 mSec when using 60Hz Video
6A	ANAPWRDN1	R/W	ISENPD	5	0	ISEN Power Down
			IDMAXPD	4	0	IDMAX Power Down
			VREFPD	3	0	VREF Power Down
			GMSENPD	2	0	Gamma Sensor Power Down
			VCSENPD	1	0	VCOM Sensor Power Down
			TREFPD	0	0	Temperature Reference Power Down
6B	ANAPWRDN2		LVDSPD	6	0	LVDS receiver Power Down
			RADCPD	5	0	RAMP ADC Power Down
			RBUFPD	4	0	RAMP Buffer Power Down
			RAMPPD	3	0	RAMP DAC AMP Power Down
			DACPD	2	0	RAMP DAC Power Down
			POR50VPD	1	0	5V POR Power Down
			POR18VPD	0	0	1.8V POR Power Down
6C	TPLINWTH	R/W		7-0	0	Line Test Pattern Line Width (0=1pixel, 1=2pixel, …, 255=256pixel)
6D	TPCOLSP	R/W		7-0	0	Line Test Pattern Column Space (0=1pixel, 1=2pixel, …., 255=256pixel)
6E	TPROWSP	R/W		7-0	0	Line Test Pattern Row Spce (0=1pixel, 1=2pixel, …, 255=256pixel)
6F	TPCOLOR	R/W		7-0	07	PATTSEL=3~6: bit 6-4 for background color (RGB) and bit 2-0 for foreground color (RGB) PATTSEL=7: All 8bits for color screen
70	DSAMPEN	R/W		0	0	LVDS Data input sampling enable 0 = Disable sampling, 1 = Enable sampling
71	PSAMP	R/O		7-0	-	LVDS clock rising edge sampling readout for RD0 ~ RD16
72				15-8		
73				16		
74	NSAMP	R/O		7-0	-	LVDS clock faling edge sampling readout for RD0 ~ RD16
75				15-8		
76				16		
77 - 88	RESERVED					Reserved for testing - Do not attempt to modify these registers as it may cause terminal damage

11. DETAILED REGISTER DESCRIPTIONS

11.1 STAT (00h)

Name	STAT
Address	00h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
REV	2-0	0	Silicon revision number; Rev. 1 = 0

Bits REV in this register indicate the revision number of the silicon backplane design, with 0 corresponding to the first silicon known as Rev. 1.

11.2 VINMODE (01h)

Name	VINMODE
Address	01h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
WRDISABLE	7	0	I^2C register write disable
N/A	6-3	0	Blank – Not used
SET_ENABLE	2	1	Automatic VSYNC/HSYNC Polarity Detection Enable
VSYNCPOL	1	1	VSYNC polarity
HYSYNCPOL	0	1	HSYNC polarity

WRDISABLE:

0 = write enable (all registers can be updated externally via I^2C) (default)
1 = write protected (all other registers become read only)

SET_ENABLE:

0 = the active state of the ENABLE input is set “low” (default)
1 = the active state of the ENABLE input is set “high”

The ENABLE input pin is used to implement 3D video modes using a single RGB source, with two consecutive frames carrying information for each eye. The microdisplay can be programmed for either an active high or low ENABLE input using the SET_ENABLE bit, allowing a single video signal to be used with two displays. In such a configuration, one display scans and displays, while the other one holds and displays. The active state of the ENABLE input corresponds to the video data being scanned and displayed by the microdisplay.

To implement the Frame Sequential 3D Mode according to the VESA Standard for Stereoscopic Display Hardware, the display for the left eye is programmed with SET_ENABLE=1 and the right eye display is programmed with SET_ENABLE=0. Consequently, the data for the left eye is supplied and displayed when ENABLE=1 while the display for the right eye displays the previous frame of data.

VSYNCPOL and HSYNCPOL are overridden by detected sync polarity when AUTOSYNC = 1.

VSYNCPOL:

0 = Negative Sync
1 = Positive Sync (default)

HSYNCPOL:

0 = Negative Sync
1 = Positive Sync (default)

The SYNCPOL registers are used to determine whether the positive or negative edge of the external synchronization clocks (HSYNC and VSYNC) is used as the active transition by the internal display sequencers and control logic.

11.3 DISPMODE (02h)

Name	DISPMODE
Address	02h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
DISPOFF	7	1	Display On/Off control
POS2EN	6	0	Select widow position register for pixel doubling mode
MONO	5	0	Mono video input/display mode
3D-MODE	4	0	3D Mode control
Reserved	3-2	0	Do not change
VSCAN	1	0	Vertical Scan direction

DISPOFF:

0 = Display is turned ON
1 = Display is turned OFF (default)

The display starts in the OFF state by default and requires a command via the serial port to be turned on.

POS2EN
0 = LFTPOS ~ BOTPOS registers are used for pixel doubled window position setting when PXLDBL=1
1 = LFTPOS2 ~ BOTPOS2 registers are used for pixel doubled window position setting when PXLDBL=1

MONO:

0 = Color display mode (default)
1 = Mono display mode

The MONO is used to set monochrome display mode. When MONO = 1, the 2K_CFXL only accept the input data from LVDS channel 4,5,6,7, 8, and 9. Other channels (channel 0 to 3 and channel 10 to16) are powered down. If the application does not make use of these channels, they can be left unconnected due to internal pull downs.

3D-MODE:

0 = Normal display mode (default)
1 = Time Sequential 3D mode

These bits are used to set the 3D mode of operation in conjunction with SET_ENABLE (bit #2 of the VINMODE register) and the Enable input. In Frame Sequential Mode, each video frame contains information for either the left or the right eye. The following description for Frame Sequential operation assumes the source complies with the VESA standard, where the data for the left eye is provided while the Enable signal is at the logic high level, and the data for the right eye display is provided while the Enable signal is at the logic low level. The Enable input signal is sampled into the circuit by a flip-flop clocked on the falling edge of VSYNC and the sampled value is used for the next frame. (The Enable signal is generated by the graphics software and may not be synchronized to the VSYNC signal).

To activate the stereovision mode, the right eye display needs to be configured with Enable active low (SET_ENABLE= "0", bit #3 of the VINMODE register). This will allow the right eye microdisplay to hold the previous frame while the Enable input is high. The left eye display needs to be configured with Enable active high (SET_ENABLE="1", bit #3 of the VINMODE register). Thus, the two Enable inputs can be tied together to the incoming Stereo Sync signal provided by the graphics adapter (or other custom source).

VSCAN:

0 = Top to Bottom vertical scan direction (default)
1 = Bottom to Top vertical scan direction

HSCAN:

0 = Left to Right horizontal scan direction (default)
1 = Right to Left horizontal scan direction

11.4 LVDSCTL (03h)

Name	LVDSCTL
Address	03h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
-	7	0	Blank – Not Used
PXLDBL	6	0	Pixel doubling mode enable 0: Normal display mode 1: Pixel doubling mode
VIDMODE	5-4	0	Video input port selection 00: Quad pixel video input 01: Dual pixel video input

			10/11: Single pixel video input
CLKDLY	3-0	2	Clock delay selection for LVDS receiver latch 0: No delay 1: One unit delay 15: 15 unit delay

PXLDBL:

0 = Normal display mode
1 = Pixel Doubling mode

4X larger pictures are displayed than input source video. An input pixel is displayed in 2X2 pixel array.

VIDMODE:

00 = Quad pixel input mode, 4 Pixels simultaneous serial transfer using all 17 LVDS data and sync. channels
01 = Dual pixel input mode, 2 pixels simultaneous serial transfer using 9 LVDS data and sync. Channels.
1X = Single pixel input mode, it use only 5 LVDS data and sync. channels

All unused LVDS ports in Dual and Single pixel mode are powered down automatically.

CLKDLY:
0 = Base delay
1 = Base + one unit delay

2 = Base + two unit delay
:
F = Base + 15 unit delay

Estimated one unit delay is 150ps, and it is applied to the internal serial data latch clock

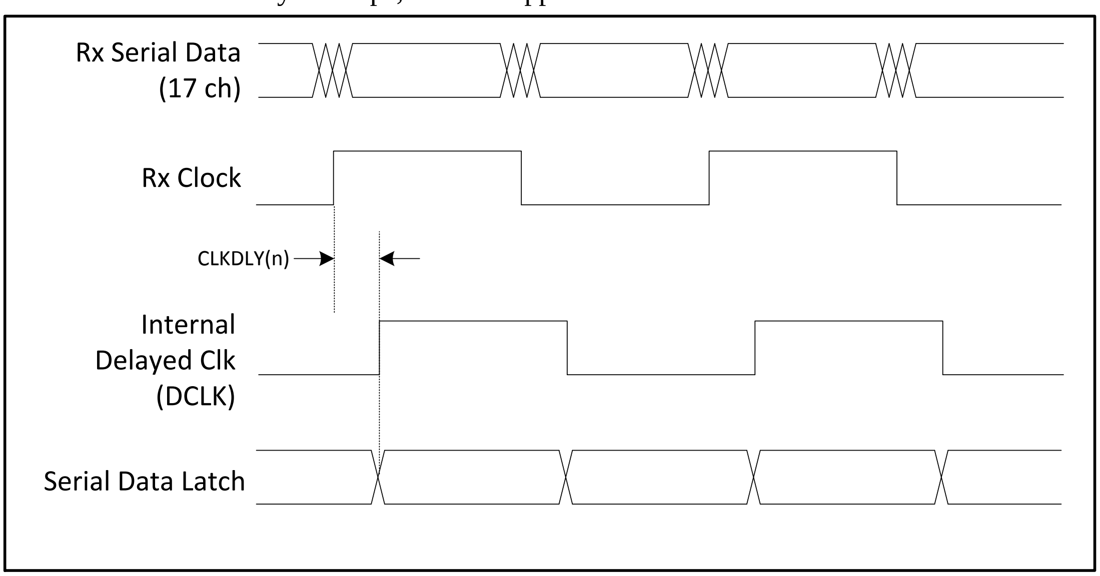


Figure 1. CLKDLY Timing Diagram

11.5 LFTPOS (04h, 05h)

Name	LFTPOS
Address	04h, 05h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LFTPOSL(04h)	7-0	0C	Left position of first active column (LSB 8bit)
LFTPOSH(05h)	10-8	0	Left position of first active column (MSB 3bit)

This register, along with register RGTPOS, is used to set the horizontal position of the active display window within the 2072 available columns of pixels. In 2K2K mode the active window can be moved by +/-12 pixels from the center (default) position. When LFTPOS is increased, register RGTPOS must be decreased by the same value so that the sum of the two remains equal.

11.6 RGTPOS (06h, 07h)

Name	RGTPOS
Address	06h, 07h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
RGTPOSL(06h)	7-0	0C	Right position of last active column (LSB 8bit)
RGTPOSH(07h)	10-8	0	Right position of last active column (MSB 3bit)

This register, along with register LFTPOS, is used to set the horizontal position of the active display window within the 2072 available columns of pixels. In 2K2K mode the active window can be moved by +/-12 pixels from the center (default) position. When RGTPOS is increased, register LFTPOS must be decreased by the same value so that the sum of the two remains equal.

11.7 TOPPOS (08h, 09h)

Name	TOPPOS
Address	08h, 09h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
TOPPOSL(08h)	7-0	0C	Top position of first active row (LSB 8bit)
TOPPOSH(09h)	10-8	0	Top position of first active row (MSB 3bit)

This register, along with register BOTPOS, is used to set the vertical position of the active display window within the 2072 available rows of pixels. In 2K2K mode the active window can be moved by +/-12 pixels from the center (default) position. When TOPPOS is increased, register BOTPOS must be decreased by the same value so that the sum of the two remains equal.

11.8 BOTPOS (0Ah, 0Bh)

Name	BOTPOS
Address	0Ah, 0Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
BOTPOSL(0Ah)	7-0	0C	Bottom position of last active row (LSB 8bit)
BOTPOSH(0Bh)	10-8	0	Bottom position of last active row (MSB 3bit)

This register, along with register TOPPOS, is used to set the vertical position of the active display window within the 2072 available rows of pixels. In 2K2K mode the active window can be moved by +/- 12 pixels from the center (default) position. When BOTPOS is increased, register TOPPOS must be decreased by the same value so that the sum of the two remains equal.

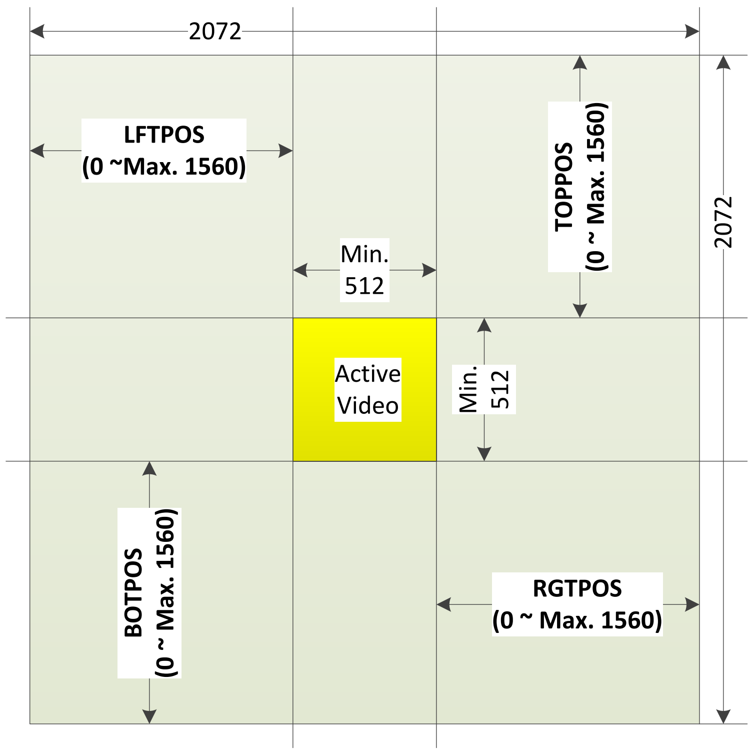


Figure 2. Picture Position Registers

The minimum active window size is limited to 512 x 512.

11.9 ROWRESET (0Ch, 0Dh)

Name	ROWRESET
Address	0Ch, 0Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ROWRESETL (0Ch)	7-0	0	Row duty rate control (LSB 8bit)
ROWRESETH (0Dh)	10-8	0	Row duty rate control (MSB 3bit)
	12	0	ROWRESET works on UNENABLED frame in 3D mode

This register is used to set the number of line cycles (in steps of 2) during which each row is active in any frame period. Each row is driven to black during the non-active line cycles.

ROWRESET (dec)	Active Line Cycles	Active Duty Rate (%)	Note
0	all	100	Pixels active for entire frame period
1	2	$2*T_{HSYNC}/T_{FRAME}$	2107 total HS cycles / frame (2K2K/60Hz)
n	2*n	$2*n*T_{HSYNC}/T_{FRAME}$	
>1053	all	100	Pixels active for entire frame period

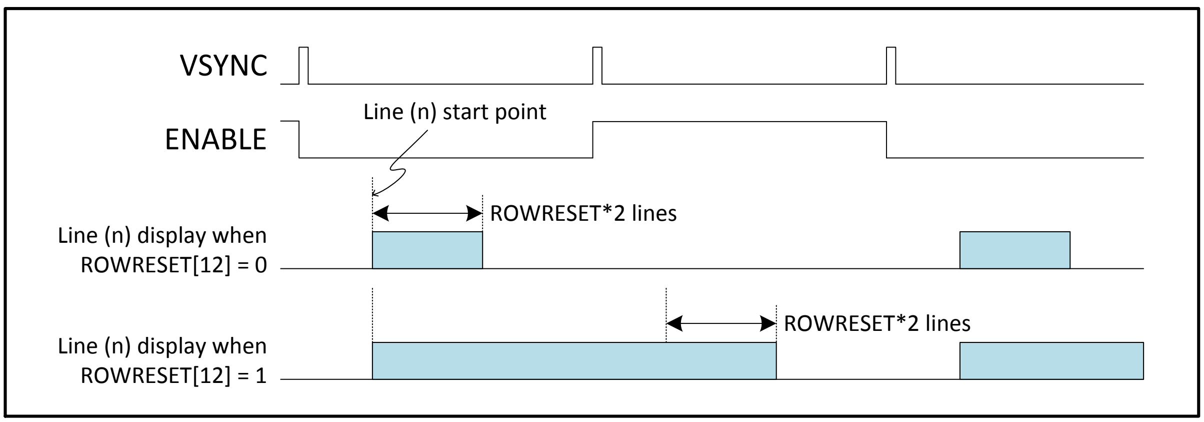


Figure 3. ROWRESET[12] Timing Diagram in 3D mode

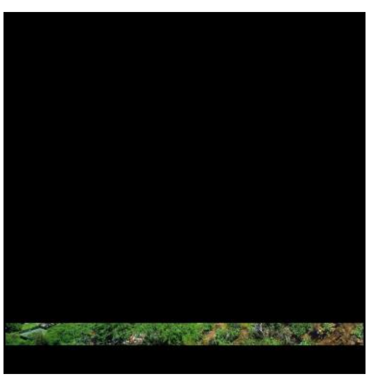


Figure 4. Example 2K 2K picture at an moment in a frame with RORESET = 040h

11.10 IDRF (0Eh)

Name	IDRF
Address	0Eh

Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
IDRF_COARSE	7-5	0	Coarse adjustment for array reference current
IDRF_FINE	4-0	01	Fine adjustment for array reference current

IDRF_COARSE:

IC#
0h = 0 (default)
1h = 0.5
2h = 1.5
3h = 2.5
4h = 3.5

IDRF_FINE:

IF#
00h = 0
01h = 1/32 (default)
…
10h = 16/32
…
1Fh = 31/32

Register IDRF is used to set the maximum OLED current, which determines the luminance level for the display. The luminance will be directly proportional to the IDRF factor (sum of IC# and IF#) and the reference luminance LDEF given by the following expression:

LMAX = LDEF*(IC# + IF#) in cd/m^2

where the luminance for a color display is LDEF ≈ 30cd/m^2 for IDRF = 30h

IDRF (hex)	LMAX / LDEF
0	0
10	0.5
20	0.5
30	1
40	1.5
50	2
60	2.5
70	3
80	3.5

11.11 DIMCTL (0Fh)

Name	DIMCTL
Address	0Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	6-0	01	Dimming level control

00h = 0
01h = 1% of LMAX
…
64h = 100% of LMAX
…
7Fh = 127% of LMAX

This register provides linear control of the display luminance level ranging from 0 to 127% in steps of 1%. The default value of 01h is equal to 1% of the luminance defined by register IDRF.

This register is only operational in Auto VCOM mode (VCOMMODE=00).

11.12 IDSTEP (10h)

Name	IDSTEP
Address	10h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
IDSTEP	2-0	0	Current level for gamma sensor

IDSTEP:

0h ≈ IDRF/128
1h ≈ IDRF/64
2h ≈ IDRF/32
3h ≈ IDRF/16
4h ≈ IDRF/8
5h ≈ IDRF/4
6h ≈ IDRF/2
7h = IDRF

The IDSTEP register is used to set the current level for the gamma sensor. The corresponding output voltage is provided at pin VGN.

A minimum of 10msec following an IDSTEP register update should be allowed for the VGN signal to settle before sampling. In addition, sampling of the VGN signal should be carried out during the Frame Blanking time.

11.13 VCOMCTL (11h)

Name	VCOMCTL
Address	11h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
VCKDUTY	4-2	3	VCOM clock duty control
VCKSEL	1-0	3	VCOM clock select

VCKDUTY:

0h = 1:7
1h = 1:3
2h = 3:5
3h = 1:1 (default)
4h = 5:3
5h = 3:1
6h = 7:1
7h = don't use

Register VCKDUTY sets the VCOM clock duty ratio (high-low).

VCKSEL:

0h = Generate Custome VCOM clock with NVCK0/NVCK1 Reg.
(See NVCK0/NVCK1 description
1h = 250 kHz
2h = 500 kHz
3h = 800 kHz (default)

Register VCKSEL sets the operating frequency of the VCOM clock.
The default setting should work for most applications. A lower frequency setting may be needed if there is excessive line noise in the image.

11.14 TEMPOUT (12h)

Name	TEMPOUT
Address	12h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
	7-0	-	Temperature sensor readout

Register TEMPOUT provides an 8bit digital output that is linearly proportional to the chip temperature. The 2K2K display temperature sensor is designed using a P-N junction. The output of the junction is sampled by an internal current to voltage converter, digitized and stored into a dedicated 8-bit register TEMPOUT. The sampling rate is controlled by configuration register TUPDATE (69H). By default the temperature sensor is updated once every 255 frames. Two registers are used to set the sensor gain (TREFDIV) and sensor offset (TEMPOFF). The temperature sensor can be powered down when not used by setting TSENPD =1 in the PWRDN register.

The temperature sensor is intended to provide a full-scale reading over a temperature range defined by the user. Assuming that the desired operating temperature range is defined by T_{MIN} and T_{MAX}, the expected sensor response would be as follows:

$$TEMPOUT(dec) = A * temp + B$$

where temp is the chip temperature in degrees Celsius, and A and B are given by:

$$A = \frac{255}{T_{MAX} - T_{MIN}}$$

$$B = \frac{-255 * T_{MIN}}{T_{MAX} - T_{MIN}}$$

The actual sensor response is determined by registers TREFDIV and TEMPOFF through the following relationship:

$$TEMPOUT(d) = k_1 * TREFDIV(d) * temp + k_2 + TEMPOFF(d)$$

The constants k_1 and k_2 are dependent on properties of the silicon and package assembly. For example, the average register settings needed to achieve a working temperature range of -60ºC to +80ºC are given by the following values for package A04-500463-01:

$$TREFDIV(d) = 25$$
$$TEMPOFF(d) = 93$$

Using these values will result in a variation in temperature reading from part to part due to manufacturing tolerances. To get a reasonably good sensor performance it is usually enough to just find the optimum value for TEMPOFF, which requires only one measurement at room temperature. Increased accuracy can be obtained for a specific part by performing the calibration measurements described below.

To find the optimum value for TREFDIV do the following:

- Place the display in a temperature controlled environment, e.g. an oven
- Set TREFDIV=25d=19h and TEMPOFF=0
- Set DISPMODE=80h (turn off the display)
- Read TEMPOFF at several ambient temperatures, e.g. 0ºC, 20ºC, 40ºC, 60ºC
- Take the slope to find the sensor response, A_{MEAS} = dTEMPOUT(d)/dtemp
- The optimum value for TREFDIV is then given by

$$TREFDIV_{OPT} = 25 * \frac{1.82}{A_{MEAS}}$$

To find the optimum value for TEMPOFF do the following:

- Set TREFDIV=25d=19h (or the optimum value) and TEMPOFF=0
- Set DISPMODE=80h (turn off the display)
- Allow several minutes to stabilize and then read $TEMPOUT_{AMB}$ and the ambient temperature T_{AMB}
- The optimum value for TEMPOFF is then given by

$$TEMPOFF_{OPT} = 1.82 * T_{AMB} + 109 - TEMPOUT_{AMB}$$

With these settings, the microdisplay temperature can be found from the sensor reading through the following relationship:

$$T(°C) = \frac{140}{255} * TEMPOUT(d) - 60$$

Temperatures below -60ºC will return a TEMPOUT reading of 0 and temperatures above +80ºC will return a hexadecimal value of FF.

11.15 PWRDOWN (13h)

Name	SYSPWRDN
Address	13h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SYSPD	4	0	All systems power down
	3-2	0	Blank
VCOMPD	1	0	VCOM power down
TSENPD	0	0	Temperature Sensor power down

SYSPD:

1 = all systems are powered down
0 = normal operation (default)

By setting the SYSPD bit to a “1”, the chip enters a deep sleep mode in which all functions in order to minimize power consumption. The data, sync and clock inputs should be inactive and held low to achieve the lowest power consumption.
All register settings are saved in the power down mode and the display will restart in its previous state when normal operation is resumed by releasing this bit via I2C.

VCOMPD:

1 = VCOM generator is powered down
0 = normal operation (default)

TSENPD:

1 = the Temperature Sensor is powered down
0 = the Temperature Sensor is operating normally (default)

11.16 TPMODE (14h)

Name	TPMODE
Address	14h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
TPVCLK	6	0	Enable external clock for Burn-In-Test-Mode
FRSEL	5-4	0	Change pattern video frame rate
PATTEN	3	0	Enable test pattern display
PATTSEL	2-0	0	Select test pattern for Burn-In mode

TPVCLK:

1 = use external video input clock for Burn-in-test pattern generator
0 = use internal ring oscillator as pattern generator clock (default)

FRSEL:

00 = select 120Hz frame rate
01 = select 80Hz frame rate
01 = select 30Hz frame rate
00 = select 60Hz frame rate (default)

FRSEL only work with internal ring oscillator mode (TPVCLK=0)

The BI pin is tied high or PATTEN register set too high to activate the Burn-In test mode, which can be used to check display functionality without the presence of external video data or clock signals. In this mode, the display generates data, syncs and the pixel clock internally for several different video patterns. The TPMODE register is used to select one of the built-in test patterns in Burn-In mode via the serial interface.

000 = all white pattern (default)
001 = color bars
010 = gray scale (without gamma correction)
011 = checkerboard pattern
100 = alternating columns pattern
101 = alternating rows pattern
110 = grid pattern
111 = gray color (8 bit gray color = TPCOLOR)

Use with registers TPLINWTH, TPCOLSP, TPROWSP and TPCOLOR to modify the patterns according to the following table.

Test Pattern Name	PATTSEL (14H:2-0)	TPLINWTH (6CH)	TPCOLSP (6DH)	TPROWSP (6EH)	TPCOLOR (6FH:2-0)	TPCOLOR (6FH:6-4)
All White	000	X	X	X	X	X

Color Bar	001	X	X	X	X	X
Gray Scale	010	X	X	X	X	X
Checker Board	011	X	X	X	X	X
Alternatin g Column	100	LW	CS	X	111	000
Alternatin g Row	101	LW	X	RS	111	000
Grid Pattern	110	LW	CS	RS	111	000
All Black	101	X	X	X	000	000
All White	101	X	X	X	111	111
All Red	101	X	X	X	100	100
All Green	101	X	X	X	010	010
All Blue	101	X	X	X	001	001

X: Don't care, LW: Line Width (0~255), CS: Column Space (0~255), RS: Row Space (0~255)

11.17 NVCK0 (15h)

Name	NVCK0
Address	15h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	06	No. of VCLK for "0" time of VcomClk when VCKSEL=0

NVCK0:

When VCKSEL =0, NVCK0 with NVCK1 are used to generate arbitrary VCOM clock frequency and duty based on the following equations.

VcomClk (Frequency) = f_{VCLK} * (1/((NVCK0+1) + (NVCK1 +1)))
VcomClk (Duty) = (NVCK1+1) / ((NVCK0+1)+(NVCK1+1))

*= f_{VCLK} is a 1/8 of the Pixel Clock of the $24_{\text{-bit}}$ RGB source video. (It correspond to the half of internal pixel clock and the internal pixel clock is ¼ of 24 bit RGB source video)

11.18 NVCK1 (16h)

Name	NVCK1

Address	16h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	99	No. of VCLK for ”1” time of VcomClk when VCKSEL=0

NVCK1:

See above NVCK0 descriptions.

11.19 VDACMX (17h)

Name	VDACMX
Address	17h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	80	RAMP DAC maximum value control

Register VDACMX is used to adjust the maximum value of the internal RAMP DAC signal by -40% to +40% of the nominal value.

NOTE: The normal operating value for VDACMX is recommended to set to 78h.

11.20 VGMAX (18h)

Name	VGMAX
Address	18h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0D	Fine adjustment for VGMAX level

00h = 5 (VAN = 5V)
0Dh = 4.95 (default)
FFh = 4

VGMAX level = VAN*(1 - 0.2*VGMAX(dec) / 255)

This register sets the pixel voltage at which the maximum OLED current is regulated. It should be slightly below the VAN supply to prevent saturation of the video buffer amplifiers.

11.21 ADVNCED (19h)

Name	ADVNCED
Address	19h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ADVNCED	0	0	Enable advanced control mode

ADVNCED:

0 = Basic control mode (default) – Registers in 60h to 88h are not accessible
1 = Advanced control mode – enables to access 60h~88h registers

11.22 LFTPOS2 (1Ah, 1Bh)

Name	LFTPOS2
Address	1Ah, 1Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LFTPOS2L(1Ah)	7-0	0C	Left position of first active column (LSB 8bit)
LFTPOS2H(1Bh)	10-8	0	Left position of first active column (MSB 3bit)

The left position of column, which is the start position of a doubled picture.

11.23 RGTPOS2 (1Ch, 1Dh)

Name	RGTPOS2
Address	1Ch, 1Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
RGTPOS2L(1Ch)	7-0	0C	Right position of last active column (LSB 8bit)
RGTPOS2H(1Dh)	10-8	0	Right position of last active column (MSB 3bit)

The right position of column in the doubled picture.

11.24 TOPPOS2 (1Eh, 1Fh)

Name	TOPPOS2
Address	1Eh, 1Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
TOPPOS2L(1Eh)	7-0	0C	Top position of first active row (LSB 8bit)
TOPPOS2H(1Fh)	10-8	0	Top position of first active row (MSB 3bit)

The top position of rows, which is a starting row in a doubled picture.

11.25 BOTPOS2 (20h, 21h)

Name	BOTPOS2
Address	20h, 21h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
BOTPOS2L(20h)	7-0	0C	Bottom position of last active row (LSB 8bit)
BOTPOS2H(21h)	10-8	0	Bottom position of last active row (MSB 3bit)

The bottom position of the rows in a doubled picture

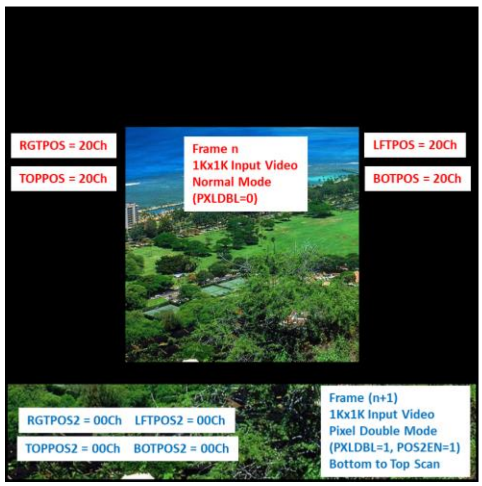


Figure 5. Transition from 1K1K native display to pixel doubled display

11.26 DISPMOD_BN (2Ah)

Name	DISPMOD_BN
Address	2Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
DISPMOD_BN	7-0	00	DISPMODE register set for Burn-in-test (replaced automatically when Burn-in mode)

When PATTEN=1 or BurnIN Pin = High, DISPMOD (02h) register is disabled and this register replace it.

11.27 IDRF_BN (2Bh)

Name	IDRF_BN
Address	2Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description

IDRF_BN	7-0	30	IDRF register set for Burn-in-test (replaced automatically when Burn-in mode)

When PATTEN=1 or BurnIN Pin = High, IDRF (0Eh) register is disabled and this register replace it.

11.28 DIMCTL_BN (2Ch)

Name	DIMCTL_BN
Address	2Ch
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
DIMCTL_BN	6-0	64	DIMCTL register set for Burn-in-test (replaced automatically when Burn-in mode)

When PATTEN=1 or BurnIN Pin = High, DIMCTL (0Fh) register is disabled and this register replace it.

11.29 LUTCTL (2Dh)

Name	LUTCTL
Address	2Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
RESERVED	7	0	Do not use
RESERVED	6-4	0	Do not use
RESERVED	3-2	0	Do not use
GAMMASEL	1-0	0	Set to 00

GAMMASEL:

00 = Manual Gamma LUT mode, use pre-characterized LUT0-7 values or a calculated LUT0-7 value by sampling VGN output using external ADC in microcontroller.

11.30 RESERVED (2Eh)

Name	RESERVED
Address	2Eh
Mode	Read / Write

Do not use this register. Reserved for internal testing

11.31 UDGAMMA

Name	UDGAMMA
Address	2Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT_UPDATE	3	0	Update LUT
LUT_RGB	2-0	7	Select R,G,B Gamma LUT for Update

LUT_UPDATE register operation

- R,G,B LUT update is started at first VSYNC rising edge after LUT_UPDATE register set to 1 for the on-the-fly update during normal operation
- LUT_UPDATE register cleared to 0 after update operation completed automatically

LUT_RGB:

001 = LUT0-7 values will be applied to BLUE data only
010 = LUT0-7 values will be applied to GREEN data only
011 = LUT0-7 values will be applied to GREEN and BLUE data
100 = LUT0-7 values will be applied to RED data only
101 = LUT0-7 values will be applied to RED and BLUE data
110 = LUT0-7 values will be applied to RED and GREEN data
111 = LUT0-7 values will be applied to all 3 colors (RED, GREEN, and BLUE data)

It is intended to allow applying different gamma characteristics to each color.

11.32 LUT0 (30h, 31h)

Name	LUT0
Address	30h, 31h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT0L (30h)	7-0	CC	LUT0 LSB 8 bit for manual Gamma LUT
LUT0H (31h)	9-8	1	LUT0 MSB 2 bit for manual Gamma LUT

The gamma correction operation is performed by a piece-wise linear interpolator using 10 bit LUT0-7 values. The 8-bit input data is converted to the 10-bit gamma corrected data for the OLED pixel. The following is an example LUTs including default values

	Input Gray	Gamma Coefficiect (LUT)			
		Default	SYSG1.5	SYSG2.0	SYSG2.5
	0	0	0	0	0
LUT0	2	460	434	335	267
LUT1	4	500	478	379	309
LUT2	8	560	514	415	345
LUT3	16	640	566	471	403
LUT4	32	740	636	548	487
LUT5	64	820	727	658	607
LUT6	128	930	847	806	777
LUT7	255	1023	1023	1023	1023

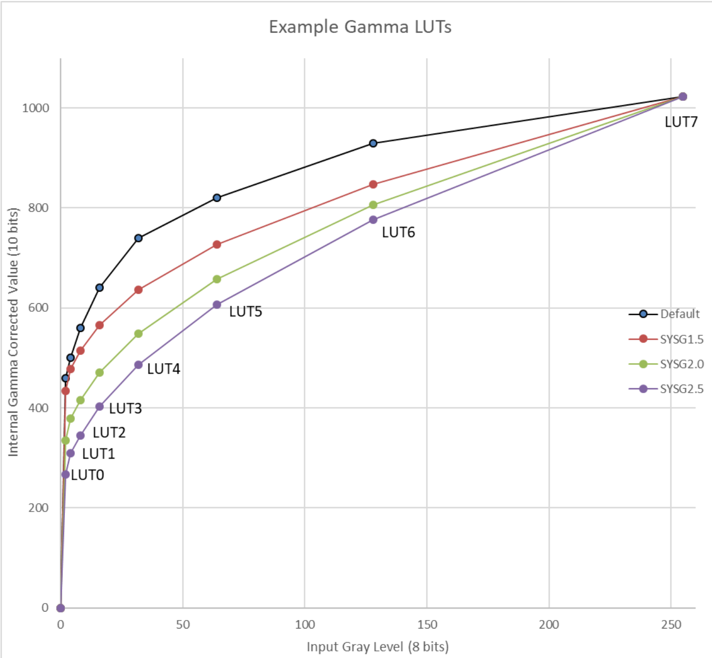


Figure 7. Gamma Correction with different set of LUT values

11.33 LUT1 (32h, 33h)

Name	LUT1
Address	32h, 33h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT1L (32h)	7-0	F4	LUT1 LSB 8 bit for manual Gamma LUT
LUT1H (33h)	9-8	1	LUT1 MSB 2 bit for manual Gamma LUT

11.34 LUT2 (34h, 35h)

Name	LUT2
Address	34h, 35h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT2L (34h)	7-0	30	LUT2 LSB 8 bit for manual Gamma LUT
LUT0H (35h)	9-8	2	LUT2 MSB 2 bit for manual Gamma LUT

11.35 LUT3 (36h, 37h)

Name	LUT3
Address	36h, 37h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT3L (36h)	7-0	80	LUT3 LSB 8 bit for manual Gamma LUT
LUT3H (37h)	9-8	2	LUT3 MSB 2 bit for manual Gamma LUT

11.36 LUT4 (38h, 39h)

Name	LUT4
Address	38h, 39h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT4L (38h)	7-0	E4	LUT4 LSB 8 bit for manual Gamma LUT
LUT4H (39h)	9-8	2	LUT4 MSB 2 bit for manual Gamma LUT

11.37 LUT5 (3Ah, 3Bh)

Name	LUT5
Address	3Ah, 3Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT5L (3Ah)	7-0	34	LUT5 LSB 8 bit for manual Gamma LUT
LUT5H (3Bh)	9-8	3	LUT5 MSB 2 bit for manual Gamma LUT

11.38 LUT6 (3Ch, 3Dh)

Name	LUT6
Address	3Ch, 3Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT6L (3Ch)	7-0	A2	LUT6 LSB 8 bit for manual Gamma LUT
LUT6H (3Dh)	9-8	3	LUT6 MSB 2 bit for manual Gamma LUT

11.39 LUT7 (3Eh, 3Fh)

Name	LUT7
Address	3Eh, 3Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LUT7L (3Eh)	7-0	FF	LUT7 LSB 8 bit for manual Gamma LUT
LUT7H (3Fh)	9-8	3	LUT7 MSB 2 bit for manual Gamma LUT

11.40 Reserved (40h – 5Fh)

Name	SGF0
Address	50h to 5Fh
Mode	Read / Write

Reserved for internal testing. Do not make changes to these registers

11.41 RAMPCTL (60h)

Name	RAMPCTL
Address	60h
Mode	Read / Write

Reserved for internal testing. Do not make changes to these registers

11.42 RAMPCM

Name	RAMPCM
Address	61h
Mode	Read / Write

Reserved for internal testing. Do not make changes to these registers

11.43 BIASN (62h)

Name	BIASN
Address	62h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
BIASCTEN	4	0	Enable BIAS control
EXT_VREF	3	0	Enable external VREF
BIASN	2-0	1	Set pixel bias current

BIASCTEN:

Reserved for internal testing. Do not make changes to this value

EXT_VREF:

Reserved for internal testing. Do not make changes to this value

BIASN:

000 = pixel bias current is turned off
001 = pixel bias current set to 0.5nA (default)
010 = pixel bias current set to 1.0 nA

011 = pixel bias current set to 1.5 nA
100 = pixel bias current set to 2 nA
101 = pixel bias current set to 2.5 nA
110 = pixel bias current set to 3.0 nA
111 = pixel bias current set to 3.5 nA

The BIASN register is used to set the sink current applied in each pixel cell. It is recommended to use the BIASN=07h setting in normal operation.

11.44 VGNSHCTL (63h)

Name	VGNSHCTL
Address	63h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
PMPCTRL	2-1	0	VCOM pump hold enable during VGN sampling
VGNSH_EN	0	0	VGN sample & hold enable

PMPCTRL:

00 = Normal operation, pump hold disabled (default)
01 = Enable pump hold during VGN sampling time
10 = Enable only VSYNC period
11 = Enable only Flyback period

The PMPCTRL register is used to disable the VCOM converter switch during the VGN sampling time to reduce noise pickup.

VGNSH_EN:

0 = Bypass the VGN sample & hold function (default)
1 = Enable the VGN sample & hold function

The VGNSH_EN register is used to activate the internal sample & hold function provided at the VGN output pin.

11.45 VCOMMODE (64h)

Name	VCOMMODE
Address	64h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ISEN_EN	3-2	1	Enable the VCOM current sensor
VCOMAUTO	1-0	0	Set internal VCOM supply mode

ISEN_EN:
00 = No sensing of VCOM current

01 = Over current Protection Mode (default). It senses the current of Rsen resistor of external VCOM circuit and controls VCOM_DRV output to protect the external FET
1x = Test Purpose

VCOMAUTO:

This register sets the operating mode of the internal VCOM dc-dc converter.

00 = AUTO1 mode (default)
01 = AUTO2 mode
10 = MANUAL mode

In the AUTO1 mode, the VCOM converter uses an internal current reference to maintain a fixed OLED current level, which is defined by registers DIMCTL and IDRF.
In the AUTO2 mode, the VCOM converter regulates the OLED current level when the VCOM supply is below a set threshold (defined by the VCOM register), and clamps the output to the threshold level when conditions call for a VCOM output above the threshold level.
In the MANUAL mode, the VCOM converter uses a voltage reference signal to maintain a fixed cathode supply voltage. The value of the cathode voltage is set by register VCOM.

11.46 VCOMCTL (65h)

Name	VCOMCTL
Address	65h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SS_BYPASS	2	0	Bypass the VCOM soft start mode
VCOMSS	1-0	1	VCOM soft start delay time

SS_BYPASS:
Test Purpose. Not allowed to change it

VCOMSS:
Test Purpose. Not allowed to change it

11.47 VCOM (66h)

Name	VCOM
Address	66h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	51	VCOM manual setting

Cathode supply as a function of VCOM setting:

VCOM(h)	FF	F0	E0	D0	C0	B0	A0	90	80	70	60	**51***	40	30

Voltage	-0.29	-0.38	-0.47	-0.59	-0.72	-0.85	-1.0	-1.2	-1.43	-1.7	-2.0	**-2.4**	-2.97	-3.68

*default value

Register VCOM[7,0] sets the fixed output level for the internal VCOM inverter when VCOMAUTO =01 or 10. There is no compensation for the variation in OLED behavior with temperature in this mode of operation. As a result, a setting at room temperature will not necessarily result in optimal contrast and the same luminance at other temperatures. The default setting (51h) will result in a cathode supply ≈ -2.3V. The typical dependency of luminance on the VCOM setting in manual mode is given in Figure 21 for a color display.

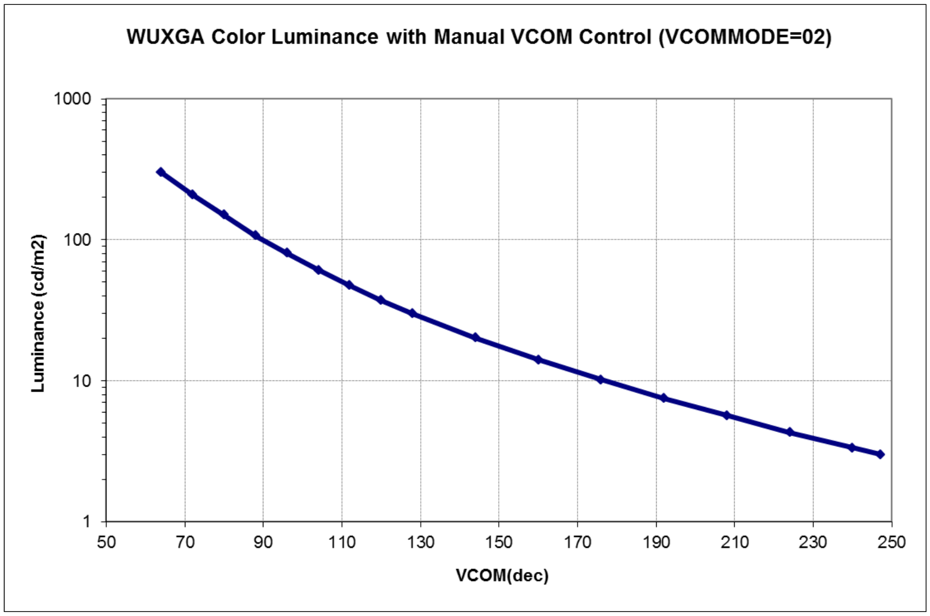


Figure 21: Typical luminance dependency on manual VCOM setting

11.48 TREFDIV (67h)

Name	TREFDIV
Address	67h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	5-0	2A	Temperature sensor reference clock divider adjust

The register TREFDIV is used to adjust the slope of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -40 to 80ºC, although the setting is best determined by a calibration measurement of the display in its final assembly.

See the description for register TEMPOUT.

11.49 TEMPOFF (68h)

Name	TEMPOFF
Address	68h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	87	Temperature sensor offset adjust

The register TEMPOFF is used to adjust the offset of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -40 to 80ºC, although the setting is best determined by a calibration measurement of the display in its final assembly.

See the description for register TEMPOUT.

11.50 TUPDATE (69h)

Name	TUPDATE
Address	69h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	FF	Number of frames per TEMPOUT update

This register sets the update rate of the Temperature Sensor reading, TEMPOUT. The time between sensor updates is given by:

$$\text{Update Time} = (\text{TUPDATE(decimal)} + 1)*T_{FRAME}$$

where the frame period T_{FRAME} is equal to 16.6 ms for 60Hz video. The valid range for TUPDATE is 02h to FFh.

11.51 ANGPWRDN1 (6Ah)

Name	ANGPWRDN
Address	6Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
ISENPD	5	0	ISEN power down
IDMAXPD	4	0	IDMAX power down
VREFPD	3	0	VREF power down
GMSENPD	2	0	Gamma sensor power down
VCSENPD	1	0	VCOM sensor power down
TREFPD	0	0	Temperature reference power down

ISENPD:

1 = VCOM current limit sensor is powered down
0 = normal operation (default)

IDMAXPD:

1 = IDMAX function is powered down
0 = normal operation (default)

VREFPD:

1 = the VREF reference source is powered down
0 = normal operation (default)

GMSENPD:

1 = the Gamma sensor is powered down
0 = normal operation (default)

VCSNEPD:

1 = the VCOM sensor is powered down
0 = normal operation (default)

TREFPD:

1 = the Temperature reference is powered down
0 = normal operation (default)

11.52 ANGPWRDN2 (6Bh)

Name	ANGPWRDN
Address	6Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
LVDSPD	6	0	LVDS receiver power down
RADCPD	5	0	RAMP ADC power down
RBUFPD	4	0	RAMP Buffer power down
RAMPPD	3	0	RAMP DAC Amp power down
DACPD	2	0	RAMP DAC power down
POR50VPD	1	0	5V POR power down
POR18VPD	0	0	1.8V POR power down

LVDSPD:

1 = LVDS receiver is powered down
0 = normal operation (default)

RADCPD:

1 = RAMP ADC is powered down
0 = normal operation (default)

RBUFPD:

1 = RAMP Buffer is powered down
0 = normal operation (default)

RAMPPD:

1 = internal RAMP DAC amplifier and buffer are powered down
0 = normal operation (default)

DACPD:

1 = internal RAMP DAC is powered down (use when external RAMP option is enabled)
0 = internal RAMP DAC is operational (default)

The internal RAMP DAC generator may be power down if an external RAMP source is used.

POR50VPD:

1 = the 5V power-on-reset circuit is powered down
0 = normal operation (default)

POR18VPD:

1 = the 1.8V power-on-reset circuit is powered down
0 = normal operation (default)

11.53 TPLINWTH (6Ch)

Name	TPLINWTH
Address	6Ch
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Test pattern line width

This register is used to set the line width for the line-type test patterns.

0 = 1 pixel wide (default)
1 = 2 pixel wide
…
255 = 256 pixel wide

11.54 TPCOLSP (6Dh)

Name	TPCOLSP
Address	6Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Test pattern column spacing

This register is used to set the column spacing for the column-type test patterns.

0 = 1 pixel space (default)
1 = 2 pixel space
…
255 = 256 pixel space

11.55 TPROWSP (6Eh)

Name	TPROWSP
Address	6Eh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Test pattern row spacing

This register is used to set the row spacing for the row-type test patterns.

0 = 1 pixel space (default)
1 = 2 pixel space
…
255 = 256 pixel space

11.56 TPCOLOR (6Fh)

Name	TPCOLOR
Address	6Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
TPCOLOR	7-0	07	Set test pattern color

This register is used to set the background and foreground colors (RGB) for certain test patterns (PATTSEL=011~101) and all 8 bit as gray color for PATTSEL=111.
When PATTSEL is 011 to 101 than bit 4 to 6 of TPCOLOR register are used as background color and bit 0 to 2 of TPCOLOR register are used as foreground color.

TPCOLOR[6:4]/TPCOLOR[2:0] when PATTSEL=011 ~ 101

000 = Black
001 = Blue
010 = Green
011 = Green & Blue
100 = Red
101 = Red & Blue
110 = Red & Green
111 = White

11.57 DSAMPEN (70h)

Name	DSAMPENR
Address	70h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
DSAMPEN	7-0	0	Test Purpose

11.58 PSAMP (71h,72h,73h)

Name	PSAMP
Address	71h,72h,73h
Mode	Read only

Bit Name	Bit#	Reset Value	Description
PSAMP (71h)	7-0	-	Test Purpose
PSAMP (72h)	15-8	-	Test Purpose
PSAMP (73h)	16	-	Test Purpose

11.59 NSAMP (74h,75h,76h)

Name	NSAMP
Address	74h,75h,76h
Mode	Read only

Bit Name	Bit#	Reset Value	Description
NSAMP (74h)	7-0	-	Test Purpose
NSAMP (75h)	15-8	-	Test Purpose
NSAMP (76h)	16	-	Test Purpose

11.60 RESERVED (77h ~ 88h)

12. TYPICAL REGISTER SETTINGS

I^2C slave address: 010011X

Address (Hex)	Name	Value (Hex)	Address (Hex)	Data	Value (Hex)	Address (Hex)	Data	Value (Hex)
0	STAT	00	30	GC4	7F	60	RAMPCTL	01
1	VINMODE	03	31	GC4	00	61	RAMPCM	44
2	DISPMODE	00	32	GC5	FF	62	BIASN	07
3	LVDSCTL	02	33	GC5	00	63	VGNSHCTL	00
4	LFTPOS	0C	34	GC6	FF	64	VCOMMODE	04
5	LFTPOS	00	35	GC6	01	65	RESERVED	00
6	RGTPOS	0C	36	GC7	FF	66	RESERVED	00
7	RGTPOS	00	37	GC7	03	67	TREFDIV	2A
8	TOPPOS	0C	38	RESERVED	00	68	TEMPOFF	87
9	TOPPOS	00	39	RESERVED	00	69	TUPDATE	FF
A	BOTPOS	0C	3A	RESERVED	00	6A	ANAPWRDN1	00
B	BOTPOS	00	3B	RESERVED	00	6B	ANAPWRDN2	00
C	ROWRESET	00	3C	RESERVED	00	6C	TPLINWTH	00
D	ROWRESET	00	3D	RESERVED	00	6D	TPCOLSP	00
E	IDRF	80	3E	RESERVED	00	6E	TPROWSP	00
F	DIMCTL	64	3F	RESERVED	00	6F	TPCOLOR	07
10	IDSTEP	00	40	RESERVED	00	70	DSAMPEN	00
11	VCOMCTL	0D	41	RESERVED	00	71	PSAMP	
12	TEMPOUT		42	RESERVED	00	72	PSAMP	
13	PWRDOWN	00	43	RESERVED	00	73	PSAMP	
14	TPMODE	00	44	RESERVED	00	74	NSAMP	
15	RESERVED	06	45	RESERVED	00	75	NSAMP	
16	RESERVED	03	46	RESERVED	00	76	NSAMP	
17	VDACMX	78	47	RESERVED	00	77	RESERVED	00
18	VGMAX	0D	48	RESERVED	00	78	RESERVED	00
19	ADVNCED	01	49	RESERVED	00	79	RESERVED	00
1A	LFTPOS2	0C	4A	RESERVED	00	7A	RESERVED	00
1B	LFTPOS2	00	4B	RESERVED	00	7B	RESERVED	00
1C	RGTPOS2	0C	4C	RESERVED	00	7C	RESERVED	00
1D	RGTPOS2	00	4D	RESERVED	00	7D	RESERVED	00
1E	TOPPOS2	0C	4E	RESERVED	00	7E	RESERVED	00
1F	TOPPOS2	00	4F	RESERVED	00	7F	RESERVED	00
20	BOTPOS2	0C	50	RESERVED	00	80	RESERVED	00
21	BOTPOS2	00	51	RESERVED	00	81	RESERVED	00
22	DISPMOD_BN	00	52	RESERVED	00	82	RESERVED	00
23	IDRF_BN	78	53	RESERVED	00	83	RESERVED	00
24	DIMCTL_BN	54	54	RESERVED	00	84	RESERVED	00
25	GMCTL	00	55	RESERVED	00	85	RESERVED	00
26	RESERVED	00	56	RESERVED	00	86	RESERVED	00
27	UDGAMMA	07	57	RESERVED	00	87	RESERVED	00
28	GC0	07	58	RESERVED	00	88	RESERVED	00
29	GC0	00	59	RESERVED	00			
2A	GC1	1F	5A	RESERVED	00			
2B	GC1	00	5B	RESERVED	00			
2C	GC2	3F	5C	RESERVED	00			
2D	GC2	00	5D	RESERVED	00			
2E	GC3	3F	5E	RESERVED	00			
2F	GC3	00	5F	RESERVED	00			

13. APPENDIX A: EXAMPLE APPLICATION SYSTEM DIAGRAM

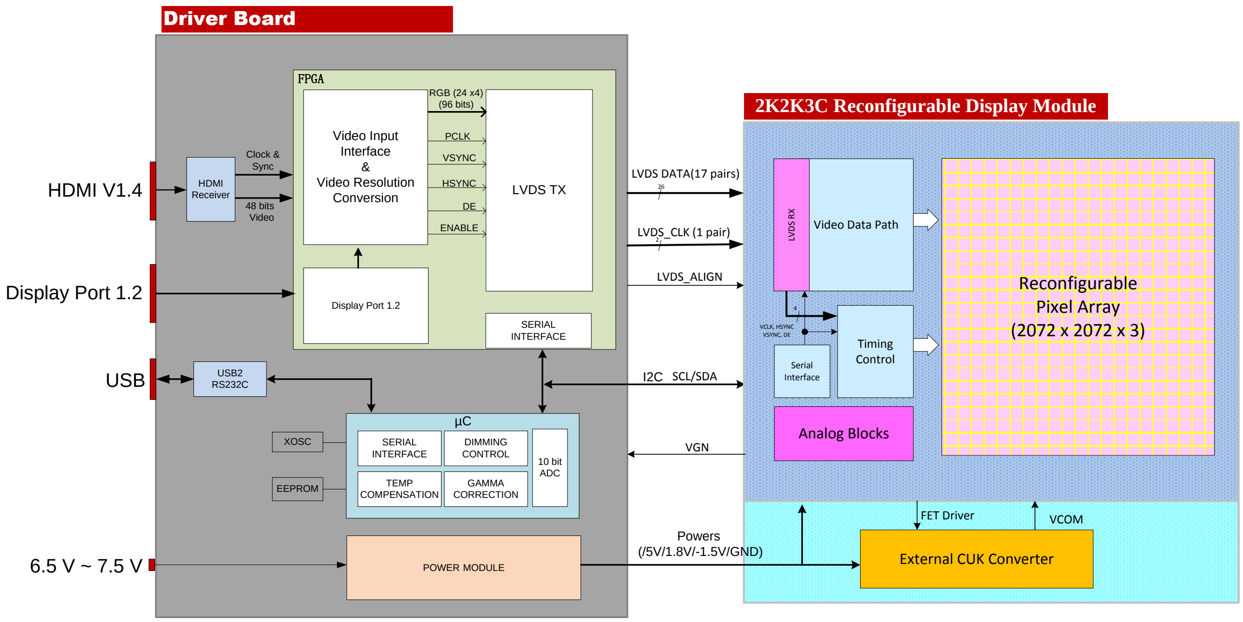


Figure A-1 Block diagram of application reference system

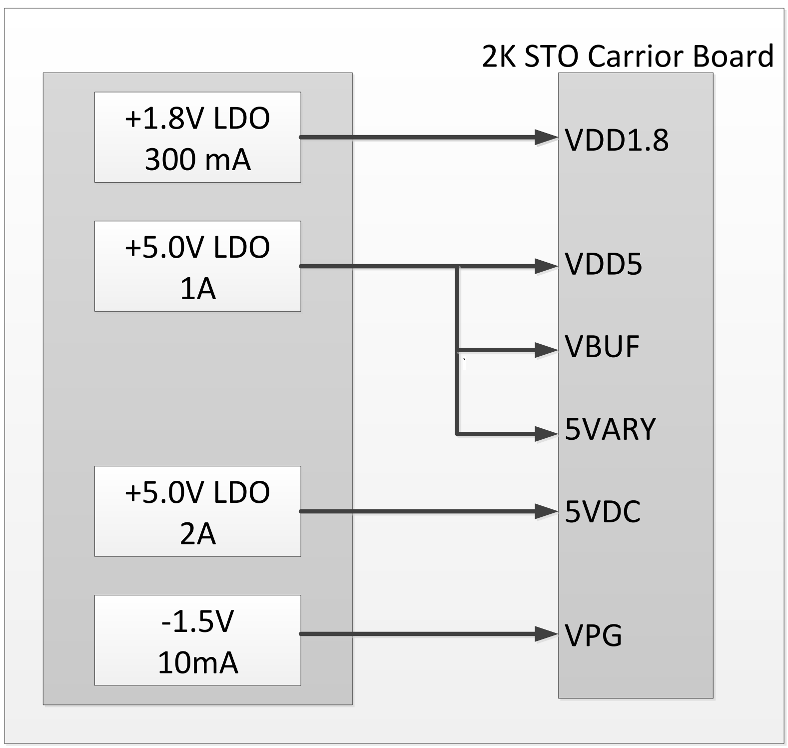


Figure A-2 Recommended Power Module

14. APPENDIX B: LVDS TRANSMITTER DESIGN EXAMPLE

The LVDS Transmitter block resides in the host system FPGA (or an independent FPGA, depending on the system design). This block encodes both data and control signals into a set of LVDS channels, according to the port mapping shown below in Table B-1. The transmitter uses a dedicated line pair for transmitting the clock signal, allowing the received to operate without a clock recovery circuit, which saves power.
The Verilog source code for this function is provided below. It is the same code as used in the eMagin Corporation Design Reference Kit FPGA.

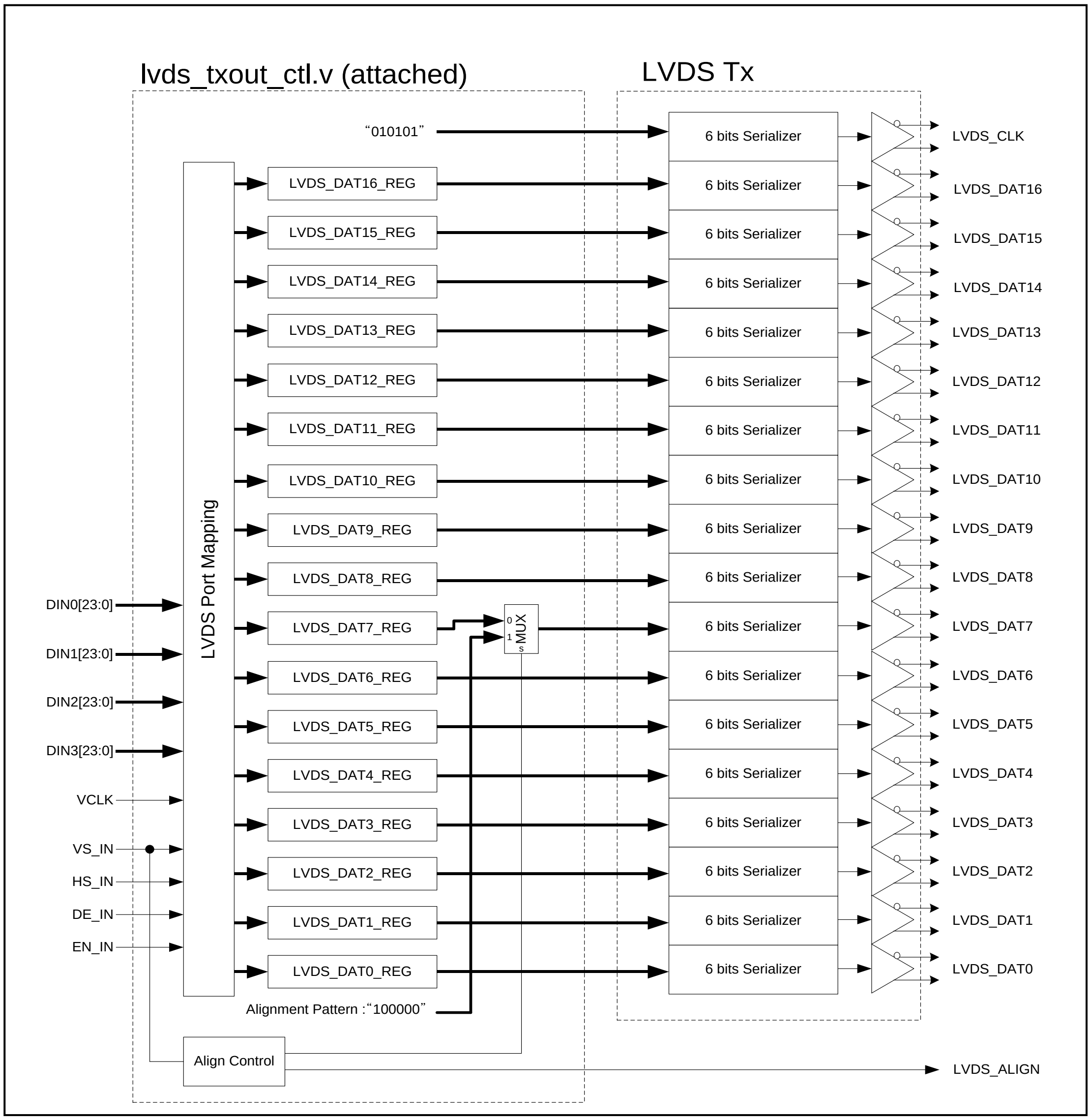


Figure B-1 : LVDS TX Reference Design

The 24 bit RGB input data to LVDS TX input data (DIN0 ~DIN3) conversion is shown below in Figure B-2. The 24 bit data need to be parallelized to 96 bit data, which reduces pixel clock by 4.

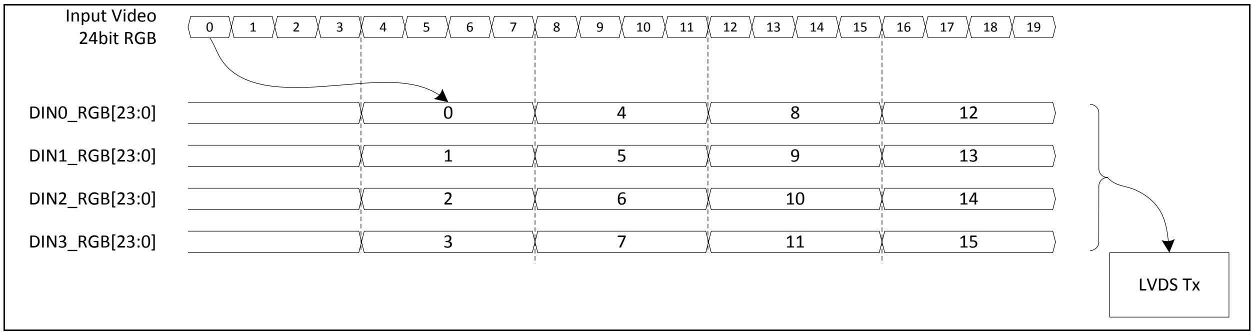


Figure B-2 : 24 bit RGB Input video to LVDS Tx data conversion for Quad Pixel transfer

In addition to encoding the data and control lines, the LVDS Transmitter also includes a logic block aimed at providing for an automatic alignment between clock and data at the receiver side (the display).

The LVDS TX (Transmitter) block, in addition of the lvds pairs, must also output the LVDS_ALGN signal (CMOS output level) to the display.

The LVDS Transmitter circuit should send the alignment pattern using the 8th LVDS data channel and send the LVDS_ALIGN signal which is CMOS output. The alignment pattern is "100000". The LVDS_ALIGN signal and align pattern should be generated during inactive video period. The Fig B-3 shows that it is generated during DE is inactive. We recommend to generate it during Vertical Blanking period.

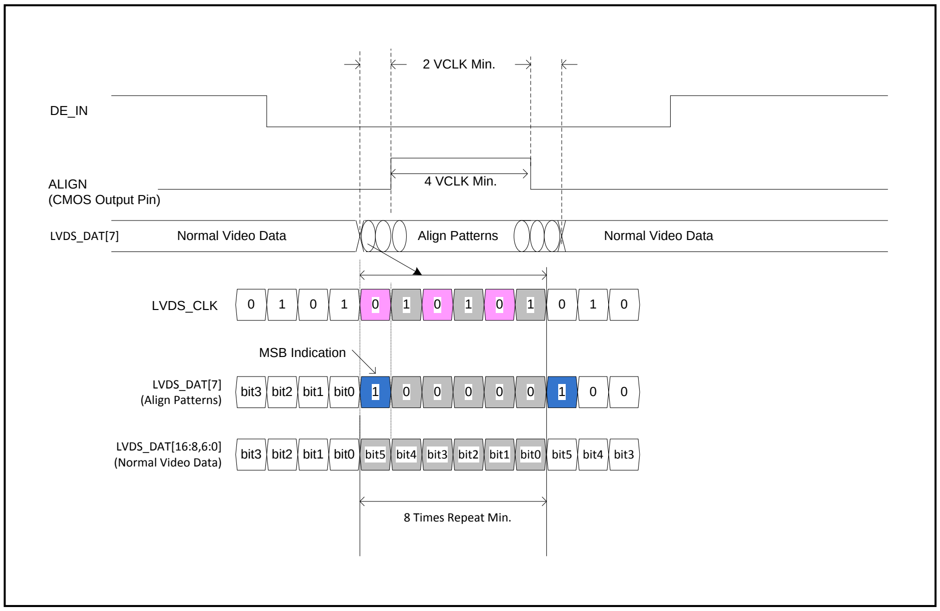


Figure B-3: LVDS Alignment Pattern and Timing

Alignment Operation

This operation is performed at power on and at periodic intervals in order to maximize signal integrity and prevent spurious noise on the display. In the eMagin Design Reference Kit and the

Verilog source code provided herein, this alignment is performed during every vertical blanking interval.
This operation is only controlled by LVDS_ALGN control signal and LVDS_ALGN signal should be generated from LVDS transmitter side with align pattern on 8th LVDS data channel.

	Bit Allocation					
LVDS Port	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
LVDS_DAT16 (RD16)	RIN3[7]	RIN3[6]	RIN3[5]	RIN3[4]	RIN3[3]	RIN3[2]
LVDS_DAT15 (RD15)	RIN3[1]	RIN3[0]	GIN3[7]	GIN3[6]	GIN3[5]	GIN3[4]
LVDS_DAT14 (RD14)	GIN3[3]	GIN3[2]	GIN3[1]	GIN3[0]	BIN3[7]	BIN3[6]
LVDS_DAT13 (RD13)	BIN3[5]	BIN3[4]	BIN3[3]	BIN3[2]	BIN3[1]	BIN3[0]
LVDS_DAT12 (RD12)	RIN1[7]	RIN1[6]	RIN1[5]	RIN1[4]	RIN1[3]	RIN1[2]
LVDS_DAT11 (RD11)	RIN1[1]	RIN1[0]	GIN1[7]	GIN1[6]	GIN1[5]	GIN1[4]
LVDS_DAT10 (RD10)	GIN1[3]	GIN1[2]	GIN1[1]	GIN1[0]	BIN1[7]	BIN1[6]
LVDS_DAT9 (RD9)	BIN1[5]	BIN1[4]	BIN1[3]	BIN1[2]	BIN1[1]	BIN1[0]
LVDS_DAT8 (RD8)	VSYNC		HSYNC		DATAEN	
LVDS_DAT7 (RD7)	RIN0[7]	RIN0[6]	RIN0[5]	RIN0[4]	RIN0[3]	RIN0[2]
LVDS_DAT6 (RD6)	RIN0[1]	RIN0[0]	GIN0[7]	GIN0[6]	GIN0[5]	GIN0[4]
LVDS_DAT5 (RD5)	GIN0[3]	GIN0[2]	GIN0[1]	GIN0[0]	BIN0[7]	BIN0[6]
LVDS_DAT4 (RD4)	BIN0[5]	BIN0[4]	BIN0[3]	BIN0[2]	BIN0[1]	BIN0[0]
LVDS_DAT3 (RD3)	RIN2[7]	RIN2[6]	RIN2[5]	RIN2[4]	RIN2[3]	RIN2[2]
LVDS_DAT2 (RD2)	RIN2[1]	RIN2[0]	GIN2[7]	GIN2[6]	GIN2[5]	GIN2[4]
LVDS_DAT1 (RD1)	GIN2[3]	GIN2[2]	GIN2[1]	GIN2[0]	BIN2[7]	BIN2[6]
LVDS_DAT0 (RD0)	BIN2[5]	BIN2[4]	BIN2[3]	BIN2[2]	BIN2[1]	BIN2[0]

Table B-1: LVDS Port Mapping for Quad Pixel Mode

Dual Pixel Transfer Mode (VIDMOD=01h)

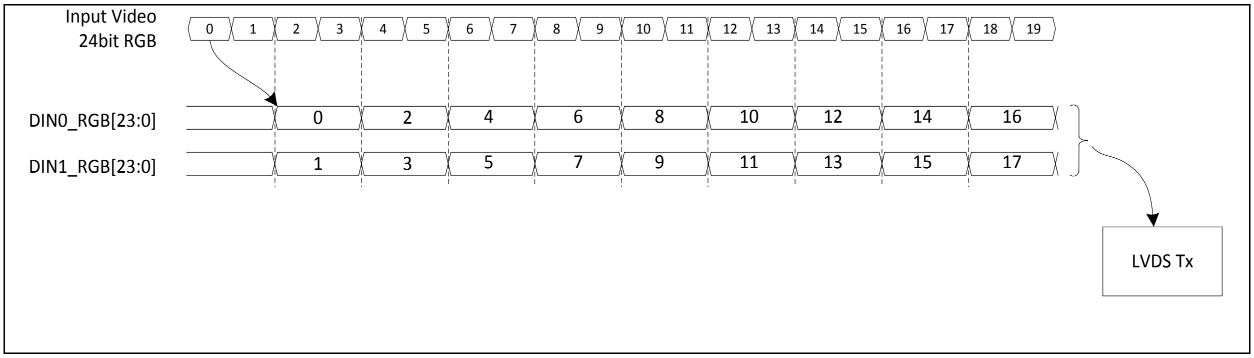


Figure B-4 : 24 bit RGB Input video to LVDS Tx data conversion for Dual Pixel transfer

		Bit Allocation					
	LVDS Port	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Not Used	*LVDS_DAT16 (RD16)*	*NC*	*NC*	*NC*	*NC*	*NC*	*NC*
	LVDS_DAT15 (RD15)	*NC*	*NC*	*NC*	*NC*	*NC*	*NC*
	LVDS_DAT14 (RD14)	*NC*	*NC*	*NC*	*NC*	*NC*	*NC*
	LVDS_DAT13 (RD13)	*NC*	*NC*	*NC*	*NC*	*NC*	*NC*
	LVDS_DAT12 (RD12)	RIN1[7]	RIN1[6]	RIN1[5]	RIN1[4]	RIN1[3]	RIN1[2]
	LVDS_DAT11 (RD11)	RIN1[1]	RIN1[0]	GIN1[7]	GIN1[6]	GIN1[5]	GIN1[4]
	LVDS_DAT10 (RD10)	GIN1[3]	GIN1[2]	GIN1[1]	GIN1[0]	BIN1[7]	BIN1[6]
	LVDS_DAT9 (RD9)	BIN1[5]	BIN1[4]	BIN1[3]	BIN1[2]	BIN1[1]	BIN1[0]
	LVDS_DAT8 (RD8)	VSYNC		HSYNC		DATAEN	
	LVDS_DAT7 (RD7)	RIN0[7]	RIN0[6]	RIN0[5]	RIN0[4]	RIN0[3]	RIN0[2]
	LVDS_DAT6 (RD6)	RIN0[1]	RIN0[0]	GIN0[7]	GIN0[6]	GIN0[5]	GIN0[4]
	LVDS_DAT5 (RD5)	GIN0[3]	GIN0[2]	GIN0[1]	GIN0[0]	BIN0[7]	BIN0[6]
	LVDS_DAT4 (RD4)	BIN0[5]	BIN0[4]	BIN0[3]	BIN0[2]	BIN0[1]	BIN0[0]
Not Used	*LVDS_DAT3 (RD3)*	*NC*	*NC*	*NC*	*NC*	*NC*	*NC*
	LVDS_DAT2 (RD2)	*NC*	*NC*	*NC*	*NC*	*NC*	*NC*
	LVDS_DAT1 (RD1)	*NC*	*NC*	*NC*	*NC*	*NC*	*NC*
	LVDS_DAT0 (RD0)	*NC*	*NC*	*NC*	*NC*	*NC*	*NC*

Table B-1: LVDS Port Mapping for Dual Pixel Mode

<u>Example RTL Code for LVDS_TXOUT_CTL.v</u>

```
//---------------------------------------------------------------------------------------------
//
// Title       : LVDS_TXOUT_CTL
// Design      : LVDS Tx Output Control Sample
// Author      : Jae Koh
// Company     : eMagin
//
//---------------------------------------------------------------------------------------------
`timescale 1ns / 1ps

module LVDS_TXOUT_18X6 ( HS_IN, rstn, DIN0, DIN1, EN_IN, EN_OUT, vclk, DOUT, DIN2,
DIN3,
        DE_IN, VS_IN, LVDS_ALGN, VSPOL );

        input [23:0] DIN0;
        input [23:0] DIN1;
        input [23:0] DIN2;
        input [23:0] DIN3;
        input vclk;
        input EN_IN;
        input VS_IN;
        input HS_IN;
        input DE_IN;
        input rstn;
        input VSPOL;

        output EN_OUT;                  // Enable Out
        output [107:0] DOUT;   // LVDS Data & VCLK Out
        output LVDS_ALGN;   // LVDS Signal Align Control

        wire EN_IN;
        wire HS_IN;
        wire [23:0] DIN0;
        wire [23:0] DIN1;
        wire [23:0] DIN2;
        wire [23:0] DIN3;
        wire vclk;
        wire VS_IN;
        wire DE_IN;
        wire rstn;
        wire VSPOL, HSPOL;

        wire EN_OUT;
        wire [107:0] DOUT;
        reg LVDS_ALGN;

        reg [107:0] DOUT0;
        reg [4:0] ENO;
        reg [8:0] VSO;
```

```
wire ALGNO;

assign EN_OUT = ENO[4];
assign DOUT = DOUT0;
assign LVDS_ALGN = VSO[3] & ~VSO[6];

assign ALGNO = VSO[0] & ~VSO[8];

wire [7:0] DINR0, DINR1, DINR2, DINR3;
wire [7:0] DING0, DING1, DING2, DING3;
wire [7:0] DINB0, DINB1, DINB2, DINB3;

assign DINR0 = DIN0[23:16];
assign DING0 = DIN0[15:8];
assign DINB0 = DIN0[7:0];
assign DINR1 = DIN1[23:16];
assign DING1 = DIN1[15:8];
assign DINB1 = DIN1[7:0];
assign DINR2 = DIN2[23:16];
assign DING2 = DIN2[15:8];
assign DINB2 = DIN2[7:0];
assign DINR3 = DIN3[23:16];
assign DING3 = DIN3[15:8];
assign DINB3 = DIN3[7:0];

always @(negedge rstn or posedge vclk)
        if (!rstn)
                begin
                        VSO <= 0;
                        ENO <= 0;
                        DOUT0 <= 0;
                end
        else
                begin
                        if (VSPOL)
                                VSO <= {VSO[7:0], VS_IN};
                        else
                                VSO <= {VSO[7:0], ~VS_IN};

                        ENO <= {ENO[3:0], EN_IN};
                        // CLKP/CLKN
                        DOUT0[107:102]          <= 6'b010101;
                        // RD16P/RD16N
                        DOUT0[101:96]           <= DINR3[7:2];
                        // RD15P/RD15N
                        DOUT0[95:90] <= {DINR3[1:0],DING3[7:4]};
                        // RD14P/RD14N
                        DOUT0[89:84] <= {DING3[3:0],DINB3[7:6]};
                        // RD13P/RD13N
                        DOUT0[83:78] <= DINB3[5:0];
                        // RD12P/RD12N
                        DOUT0[77:72] <= DINR1[7:2];
```

```
            // RD11P/RD11N
            DOUT0[71:66] <= {DINR1[1:0],DING1[7:4]};
            // RD10P/RD10N
            DOUT0[65:60] <= {DING1[3:0],DINB1[7:6]};
            // RD9P/RD9N
            DOUT0[59:54] <= DINB1[5:0];
            // RD8P/RD8N
            DOUT0[53:48] <= {VS_IN,1'b1,HS_IN,1'b1,DE_IN,1'b1};
            // RD7P/RD7N
            if (ALGNO)
                DOUT0[47:42] <= 6'b100000;
            else
                DOUT0[47:42] <= DINR0[7:2];
            // RD6P/RD6N
            DOUT0[41:36] <= {DINR0[1:0],DING0[7:4]};
            // RD5P/RD5N
            DOUT0[35:30] <= {DING0[3:0],DINB0[7:6]};
            // RD4P/RD4N
            DOUT0[29:24] <= DINB0[5:0];
            // RD3P/RD3N
            DOUT0[23:18] <= DINR2[7:2];
            // RD2P/RD2N
            DOUT0[17:12] <= {DINR2[1:0],DING2[7:4]};
            // RD1P/RD1N
            DOUT0[11:6]  <= {DING2[3:0],DINB2[7:6]};
            // RD0P/RD0N
            DOUT0[5:0]   <= DINB2[5:0];
        end
endmodule
```

15. APPENDIX C: EEPROM MEMORY MAP – (No data included with Rev A devices)

Address (Hex)	Data	Address (Hex)	Data	Address (Hex)	Data	Address (Hex)	Data
0	Serial Char #0	30	BOTPOS2	60	RESERVED	90	RESERVED
1	Serial Char #1	31	DISPMOD_	61	RESERVED	91	RESERVED
2	Serial Char #2	32	IDRF_BN	62	RESERVED	92	RESERVED
3	Serial Char #3	33	DIMCTL_BN	63	RESERVED	93	RESERVED
4	Serial Char #4	34	GMCTL	64	RESERVED	94	RESERVED
5	Lot Char#0	35	RESERVED	65	RESERVED	95	RESERVED
6	Lot Char#1	36	UDGAMMA	66	RESERVED	96	RESERVED
7	Lot Char#2	37	GC0	67	RESERVED	97	RESERVED
8	Lot Char#3	38	GC0	68	RESERVED	98	VGNA0_HI
9	Lot Char#4	39	GC1	69	RESERVED	99	VGNA0_LO
A	Lot Char#5	3A	GC1	6A	RESERVED	9A	VGNA1_HI
B	Wafer Char#0	3B	GC2	6B	RESERVED	9B	VGNA1_LO
C	Wafer Char#1	3C	GC2	6C	RESERVED	9C	VGNA2_HI
D	Wafer Char#2	3D	GC3	6D	RESERVED	9D	VGNA2_LO
E	Wafer Char#3	3E	GC3	6E	RESERVED	9E	VGNA3_HI
F	STAT	3F	GC4	6F	RAMPCTL	9F	VGNA3_LO
10	VINMODE	40	GC4	70	RAMPCM	A0	VGNA4_HI
11	DISPMODE	41	GC5	71	BIASN	A1	VGNA4_LO
12	LVDSCTL	42	GC5	72	VGNSHCTL	A2	VGNA5_HI
13	LFTPOS	43	GC6	73	VCOMMODE	A3	VGNA5_LO
14	LFTPOS	44	GC6	74	RESERVED	A4	VGNA6_HI
15	RGTPOS	45	GC7	75	RESERVED	A5	VGNA6_LO
16	RGTPOS	46	GC7	76	TREFDIV	A6	VGNA7_HI
17	TOPPOS	47	RESERVED	77	TEMPOFF	A7	VGNA7_LO
18	TOPPOS	48	RESERVED	78	TUPDATE	A8	VGNB0_HI
19	BOTPOS	49	RESERVED	79	ANAPWRDN1	A9	VGNB0_LO
1A	BOTPOS	4A	RESERVED	7A	ANAPWRDN2	AA	VGNB1_HI
1B	ROWRESET	4B	RESERVED	7B	TPLINWTH	AB	VGNB1_LO
1C	ROWRESET	4C	RESERVED	7C	TPCOLSP	AC	VGNB2_HI
1D	IDRF	4D	RESERVED	7D	TPROWSP	AD	VGNB2_LO
1E	DIMCTL	4E	RESERVED	7E	TPCOLOR	AE	VGNB3_HI
1F	IDSTEP	4F	RESERVED	7F	DSAMPEN	AF	VGNB3_LO
20	VCOMCTL	50	RESERVED	80	PSAMP	B0	VGNB4_HI
21	TEMPOUT	51	RESERVED	81	PSAMP	B1	VGNB4_LO
22	PWRDOWN	52	RESERVED	82	PSAMP	B2	VGNB5_HI
23	TPMODE	53	RESERVED	83	NSAMP	B3	VGNB5_LO
24	RESERVED	54	RESERVED	84	NSAMP	B4	VGNB6_HI
25	RESERVED	55	RESERVED	85	NSAMP	B5	VGNB6_LO
26	VDACMX	56	RESERVED	86	RESERVED	B6	VGNB7_HI
27	VGMAX	57	RESERVED	87	RESERVED	B7	VGNB7_LO
28	ADVNCED	58	RESERVED	88	RESERVED	B8	MM
29	LFTPOS2	59	RESERVED	89	RESERVED	B9	DD
2A	LFTPOS2	5A	RESERVED	8A	RESERVED	BA	YY
2B	RGTPOS2	5B	RESERVED	8B	RESERVED	BB	YY
2C	RGTPOS2	5C	RESERVED	8C	RESERVED	BC	slope1 (int)
2D	TOPPOS2	5D	RESERVED	8D	RESERVED	BD	slope2 (frac)
2E	TOPPOS2	5E	RESERVED	8E	RESERVED	BE	Intercept_LO
2F	BOTPOS2	5F	RESERVED	8F	RESERVED	BF	Intercept_HI