

SXGA

1280 X 1024 LOW POWER COLOR AMOLED MICRODISPLAY



DATASHEET *Revision 10*

For Part Numbers:

EMA-100502 (color)
EMA-100503 (monochrome white)
EMA-100504 (monochrome green)

eMagin Corporation reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other rights. Application circuits shown, if any, are typical examples illustrating the operation of the devices. eMagin Corporation cannot assume responsibility for any problem arising out of the use of these circuits

Revision Level	Date	Scope
1	07-2008	Initial release
2	08-2008	Updated for SXGA Rev1B silicon
3	10-2008	Updated for SXGA Rev2 silicon
4	3-2009	Updated for auto-gamma function and new package
5	3-2010	Updated mechanical drawing Clarification of SCLK requirement for serial interface Updated auto-gamma description Updated Table 4-1 (pinout)
6	9-2010	Updated section 10.1.1 on Gamma Correction Updated section 10.4.5 on Gamma Sensor Updated IDRf (12.16) and DIMCTL (12.17) specifications Updated section 10.4.4 on Luminance Control Updated section 10.7 on Power-On Sequence Added Cleaning and Handling Section (9) Updated Optical Characteristics Tables (7-1, 7-2, 7-3) Added Bill of Materials (Appendix C)
7	3-2011	Updated timing diagram 6.1.1
8	6-2011	Added: <ul style="list-style-type: none"> - Mention of burn-in in section 7 - Non volatile memory information (Appendix E) - Flammability information in section 8 - Updated CIE information in section 7 - Section 9.7 System Integration Updated: <ul style="list-style-type: none"> - Mechanical drawing - Schematic drawing - Bill of materials - Product photos
9	10-2011	Updated EEPROM data (Appendix E) Updated mechanical drawing
10	10-2011	Updated mechanical drawing

TABLE OF CONTENTS

1. INTRODUCTION.....5

2. GENERAL DESCRIPTION – EMA-100502.....6

2.1 EMA-100502 SXGA COLOR XL MICRODISPLAY6

2.2 EMA-100503 SXGA MONOCHROME WHITE XL MICRODISPLAY7

2.3 EMA-100504 SXGA MONOCHROME GREEN XL MICRODISPLAY8

3. FUNCTIONAL OVERVIEW9

4. INPUT / OUTPUT DESCRIPTION.....11

5. PIXEL ARRAY LAYOUT12

6. ELECTRICAL CHARACTERISTICS.....13

6.1 TIMING CHARACTERISTICS.....15

6.1.1 *Interface Timing Diagrams*.....15

6.1.2 *DVGA Mode Timing Diagram*.....17

6.1.3 *Gamma Sensor Timing Diagram*.....17

7. OPTICAL CHARACTERISTICS.....18

8. MECHANICAL CHARACTERISTICS.....21

9. CLEANING HANDLING AND STORAGE RECOMMENDATIONS.....24

9.1 CLEANING24

9.2 GENERAL HANDLING CONSIDERATIONS.....24

9.3 STATIC CHARGE PREVENTION.....24

9.4 PROTECTION FROM DUST AND DIRT.....25

9.5 SHORT TERM STORAGE25

9.6 LONG TERM STORAGE.....25

9.7 SYSTEM INTEGRATION25

10. DETAILED FUNCTIONAL DESCRIPTION.....26

10.1 VIDEO INPUT INTERFACE.....26

10.1.1 *Gamma Correction*26

10.1.2 *Gray Code Format*.....28

10.1.3 *Row Data Expansion*.....29

10.2 D/A CONVERSION29

10.3 FORMAT AND TIMING CONTROL30

10.3.1 *Interlaced Mode*.....31

10.3.2 *Stereovision*.....32

10.4 SENSOR FUNCTIONS33

10.4.1 *Temperature Readout*.....33

10.4.2 *Luminance Regulation Sensor*.....33

10.4.3 *Pixel Bias Sensor*34

10.4.4 *Luminance Control (Dimming)*.....34

10.4.5 *Gamma Correction Sensor*.....35

10.5 DC-DC CONVERTER39

10.6 I²C SERIAL INTERFACE.....40

10.7 POWER-ON SEQUENCE42

10.8 POWER-SAVINGS MODE.....44

10.8.1	Display-Off Function	45
11.	REGISTER MAP SUMMARY	46
12.	DETAILED REGISTER DESCRIPTIONS.....	48
12.1	STAT (00H)	48
12.2	VINMODE (01H)	48
12.3	DISPMODE (02H).....	49
12.4	TOPPOS (03H)	51
12.5	BOTPOS (04H).....	51
12.6	RAMPCTL (05H)	52
12.7	RAMPCM (06H).....	52
12.8	DAOFFSET (07H)	54
12.9	EXTRAMPCTL (08H).....	55
12.10	PWSAVE (09H).....	55
12.11	BIASN (0AH)	56
12.12	GAMMASET (0BH).....	56
12.13	VCOMMODE (0CH).....	57
12.14	VGMAX (0DH)	57
12.15	VCOM (0EH).....	58
12.16	IDRF (0FH).....	59
12.17	DIMCTL (10H).....	60
12.18	TREFDIV (11H)	60
12.19	TEMPOFF (12H)	61
12.20	TUPDATE (13H).....	61
12.21	TEMPOUT (14H)	61
12.22	PWRDWN (15H).....	63
12.23	TPMODE (16H).....	65
12.24	ANATEST (17H).....	65
13.	APPENDIX A: APPLICATION SYSTEM DIAGRAM.....	66
14.	APPENDIX B: MICRODISPLAY CARRIER BOARD.....	67
15.	APPENDIX C: MICRODISPLAY ASSEMBLY BILL OF MATERIALS.....	68
16.	APPENDIX D: TYPICAL REGISTER SETTING	69
17.	APPENDIX E: EEPROM MEMORY MAP.....	70

1. INTRODUCTION

The SXGA XL device from eMagin Corporation is an active-matrix organic light emitting diode (AMOLED) microdisplay intended for near-to-eye applications that demand high resolution, high image quality, compact size, and very low power. Combining a total of 4,015,536 active dots, the SXGA display is built on a single crystal silicon backplane and features eMagin's proprietary thin-film OLED XL technology offering extended life and luminance performance.

Part number EMA-100502 refers to the color SXGA microdisplay, part number EMA-100503 refers to the monochrome white version, and part number EMA-100504 refers to the monochrome green version. These parts are functionally and mechanically identical in all other respects. Unless otherwise noted, all details in this document will refer to the color version.

The active array is comprised of 1292 x 1036 square pixels with a 12-micron pitch and a 69% fill factor. An extra 12 columns and 12 rows (beyond the 1280 x 1024 main array) are provided to enable the active SXGA display to be shifted by steps of 1 or 2 pixels in the X and Y directions for optical alignment purposes. Additional dummy and test pixels surround the active array. Each full pixel is laid out as three 4 x 12 micron identical sub-pixels, which together form the 12-micron square RGB color group. Three primary color filter stripes are applied in alignment with the sub-pixels on a white-emissive OLED layer to form the color display.

The SXGA design features eMagin's proprietary "Deep Black" architecture that ensures off-pixels are truly black, automatically optimizes contrast under all conditions, and delivers improved pixel uniformity. Video data is received via an extended 30-bit digital RGB interface with external synchronization and clocks, and the display includes on-chip digital to analog conversion, automatic luminance regulation over the full temperature range, automatic gamma correction, and programmable brightness.

The SXGA display system provides broad versatility and flexibility for the user through application of a separate FPGA driver IC or integration of drive logic into the user's electronics using eMagin provided source code. The driver IC provides control over gamma, color balance, contrast, brightness, electronic optical alignment, and video formatting.

In addition, the SXGA display carrier board also includes a non-volatile memory component, accessible via the I2C serial bus. This component contains the preferred register settings for the SXGA microdisplay.

Detailed device specifications and application information for the SXGA XL microdisplay produced by eMagin Corporation are provided in this document.

2. GENERAL DESCRIPTION – EMA-100502

2.1 EMA-100502 SXGA Color XL Microdisplay

Parameter	Specification ¹
Display Type	Emissive, Color Active Matrix Organic Light Emitting Diode on Silicon
Format	1280 (x3) x 1024 pixels
Total Pixel Array	1292 (x3) x 1036 pixels
Color Pixel Aspect Ratio	12 micron square color group
Color Pixel Arrangement	R, G, B Vertical Stripe (4 x 12 micron per sub-pixel)
Display Area	15.50 x 12.43 mm (19.87 mm diagonal, 0.78")
Useable Display Area	15.36 x 12.29 mm (19.67 mm diagonal, 0.77")
Mechanical Envelope	22.9 x 16.4 x 4.72 mm (rigid carrier board)
Weight	~ 2.5 grams
Gray Levels	256 per primary color
Uniformity	> 85% end to end
Contrast Ratio	> 10,000:1 typical
Dimming Ratio	> 400:1 with CR> 1,000:1 typical
Luminance	≥ 150 cd/m ² (front luminance), SXGA 60Hz VESA mode
Video Interface	10-bit RGB Digital, 1.8 to 2.5V CMOS
Video Source Clock	135 MHz maximum (VESA mode), up to 85Hz frame rate
Control & Serial Interface	Digital 2.5V CMOS
Power Interface	
IO/Front-end Supply (VDD)	2.5 Volts DC @ 20 mA maximum
Array/Analog Supply ² (VAN)	5.0 Volts DC @ 50 mA maximum
Bias Supply (VPG)	-1.5 Volts DC @ 1 nA maximum
Operating Ambient Temperature	-46°C to +70°C
Storage Temperature	-55°C to +90°C
Humidity	85%RH non-condensing

Note 1: The above data represents consumer and commercial performance specifications, measured at 20°C.

Note 2: Includes internally generated negative cathode supply.

2.2 EMA-100503 SXGA Monochrome White XL Microdisplay

Parameter	Specification ¹
Display Type	Emissive, White Active Matrix Organic Light Emitting Diode on Silicon
Format	1280 (x3) x 1024 pixels
Total Pixel Array	1292 (x3) x 1036 pixels
Pixel Aspect Ratio	12 micron square group
Sub-Pixel Arrangement	Vertical Stripe (4 x 12 micron per sub-pixel)
Display Area	15.50 x 12.43 mm (19.87 mm diagonal, 0.78")
Useable Display Area	15.36 x 12.29 mm (19.67 mm diagonal, 0.77")
Mechanical Envelope	22.9 x 16.4 x 4.72 mm (rigid carrier board)
Weight	~ 2.5 grams
Gray Levels	256
Uniformity	≥ 85% end to end
Contrast Ratio	> 10,000:1 typical
Dimming Ratio	> 400:1 with CR> 1,000:1 typical
Luminance	≥ 900 cd/m ² (front luminance), SXGA 60Hz VESA mode
Video Interface	10-bit (x3, 1 channel per sub-pixel) Digital, 1.8 to 2.5V CMOS
Video Source Clock	135 MHz maximum (VESA mode), up to 85Hz frame rate
Control & Serial Interface	Digital 2.5V CMOS
Power Interface	
IO/Front-end Supply (VDD)	2.5 Volts DC @ 20 mA maximum
Array/Analog Supply ² (VAN)	5.0 Volts DC @ 50 mA maximum
Bias Supply (VPG)	-1.5 Volts DC @ 1 nA maximum
Operating Ambient Temperature	-46°C to +70°C
Storage Temperature	-55°C to +90°C
Humidity	85%RH non-condensing

Note 1: The above data represents consumer and commercial performance specifications, measured at 20°C.

Note 2: Includes internally generated negative cathode supply.

2.3 EMA-100504 SXGA Monochrome Green XL Microdisplay

Parameter	Specification ¹
Display Type	Emissive, White Active Matrix Organic Light Emitting Diode on Silicon
Format	1280 (x3) x 1024 pixels
Total Pixel Array	1292 (x3) x 1036 pixels
Pixel Aspect Ratio	12 micron square group
Sub-Pixel Arrangement	Vertical Stripe (4 x 12 micron per sub-pixel)
Display Area	15.50 x 12.43 mm (19.87 mm diagonal, 0.78")
Useable Display Area	15.36 x 12.29 mm (19.67 mm diagonal, 0.77")
Mechanical Envelope	22.9 x 16.4 x 4.72 mm (rigid carrier board)
Weight	~ 2.5 grams
Gray Levels	256
Uniformity	≥ 85% end to end
Contrast Ratio	> 10,000:1 typical
Dimming Ratio	> 400:1 with CR> 1,000:1 typical
Luminance	≥ 1500 cd/m ² (front luminance), SXGA 60Hz VESA mode
Video Interface	10-bit (x3, 1 channel per sub-pixel) Digital, 1.8 to 2.5V CMOS
Video Source Clock	135 MHz maximum (VESA mode), up to 85Hz frame rate
Control & Serial Interface	Digital 2.5V CMOS
Power Interface	
IO/Front-end Supply (VDD)	2.5 Volts DC @ 20 mA maximum
Array/Analog Supply ² (VAN)	5.0 Volts DC @ 50 mA maximum
Bias Supply (VPG)	-1.5 Volts DC @ 1 nA maximum
Operating Ambient Temperature	-46°C to +70°C
Storage Temperature	-55°C to +90°C
Humidity	85%RH non-condensing

Note 1: The above data represents consumer and commercial performance specifications, measured at 20°C.

Note 2: Includes internally generated negative cathode supply.

3. FUNCTIONAL OVERVIEW

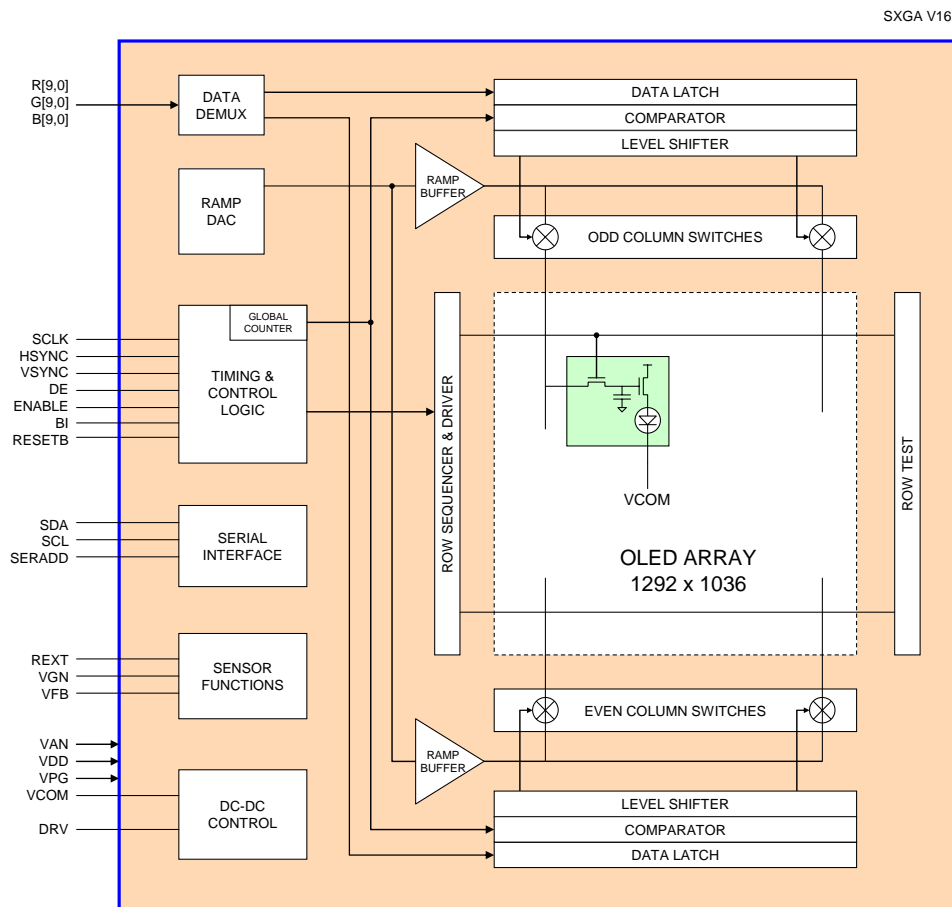


Figure 1 : SXGA design block diagram

The top-level block diagram for the SXGA microdisplay is shown in Figure 1. Bi-directional row and column sequencer circuits are used for addressing individual cells within the 1292 x 1036 x 3 pixel array, and internal digital-to-analog conversion circuits are included for converting the digital input data into the analog signals needed for programming the pixels. A storage element (capacitor) resides at each pixel cell that is used to set the gray level.

The digital video input data is applied individually to each of the three RGB sub-pixels of the color group in color mode. The RGB data inputs that make up the digital data port are configured as three 10-bit data busses. For the monochrome white version, the three 10-bit data inputs can be driven in parallel from a single 10-bit gamma corrected source, or independently with the same data. Each display pixel is made of 3 identical sub-pixels, thereby providing a triple redundancy at the pixel level.

Odd columns are driven by data sequencers located at the top of the array and even columns by bottom side sequencers. To obtain a linear gray-scale response from the OLED pixels the digital input data must be formatted with Gamma correction.

The pixel clock and sync signals for various video formats are supplied externally and converted into individual control signals by the internal timing logic block. To simplify the external driving requirements, several video formats are supported by the sequencer circuits including SXGA, HD720, and DVGA (in both progressive and interlaced modes).

The sensor block provides a number of signals for setting and regulating the display operation. These include a digital readout of the on-chip temperature, a reference level for maintaining constant luminance over temperature, a gamma correction feedback signal, and internal reference levels used for programming luminance over a wide range.

An on-chip dc-to-dc converter controller allows for the generation of the OLED cathode supply, relying on a few external passive components. The converter is an adjustable inverter that converts VAN to a negative supply used to bias the cathodes connected in common for all the array pixels via the VCOM input.

The 2-wire serial interface is a slave only I²C compatible controller with a programmable address via an external pin (LSB). The interface provides access (read and write) to on chip registers. The registers will allow the display to be configured for its various video modes and associated clock parameters. Additional control settings include luminance control, image orientation and position, internal vs. external function selection, self-test mode and various sensor settings.

The RESETB pin provides an asynchronous hardware reset function. When this pin is set to zero the display will turn off and the internal registers will be reset to their default state. After this pin is released (set to VDD) bit DISPOFF in register DISPMODE must be set high in order for the display to turn-on. If unused, this pin may be left unconnected.

The display also includes extensive functionality to support test and manufacturability including scantest for the logic blocks, row/column continuity test, JTAG pad continuity test, and a built-in test pattern generator.

Table 3-1 : SXGA Microdisplay Video Formats

Format (columns x rows)	Name	Input Mode	Output (Display) Mode
1280 x 1024 Color	SXGA	Progressive Scan	Progressive Scan
1280 x 720 Color	HD720	Progressive Scan	Progressive Scan
640 x 480 Color	DVGA	Progressive Scan	Progressive Scan (Line and Pixel doubling)
1280 x 1024 Color	SXGA 3D	Frame Sequential	Frame Sequential 3D
1280 x 720 Color	HD720 3D	Frame Sequential	Frame Sequential 3D
640 x 480 Color	DVGA	Interlaced	Interlaced Scan (Line and Pixel doubling)

4. INPUT / OUTPUT DESCRIPTION

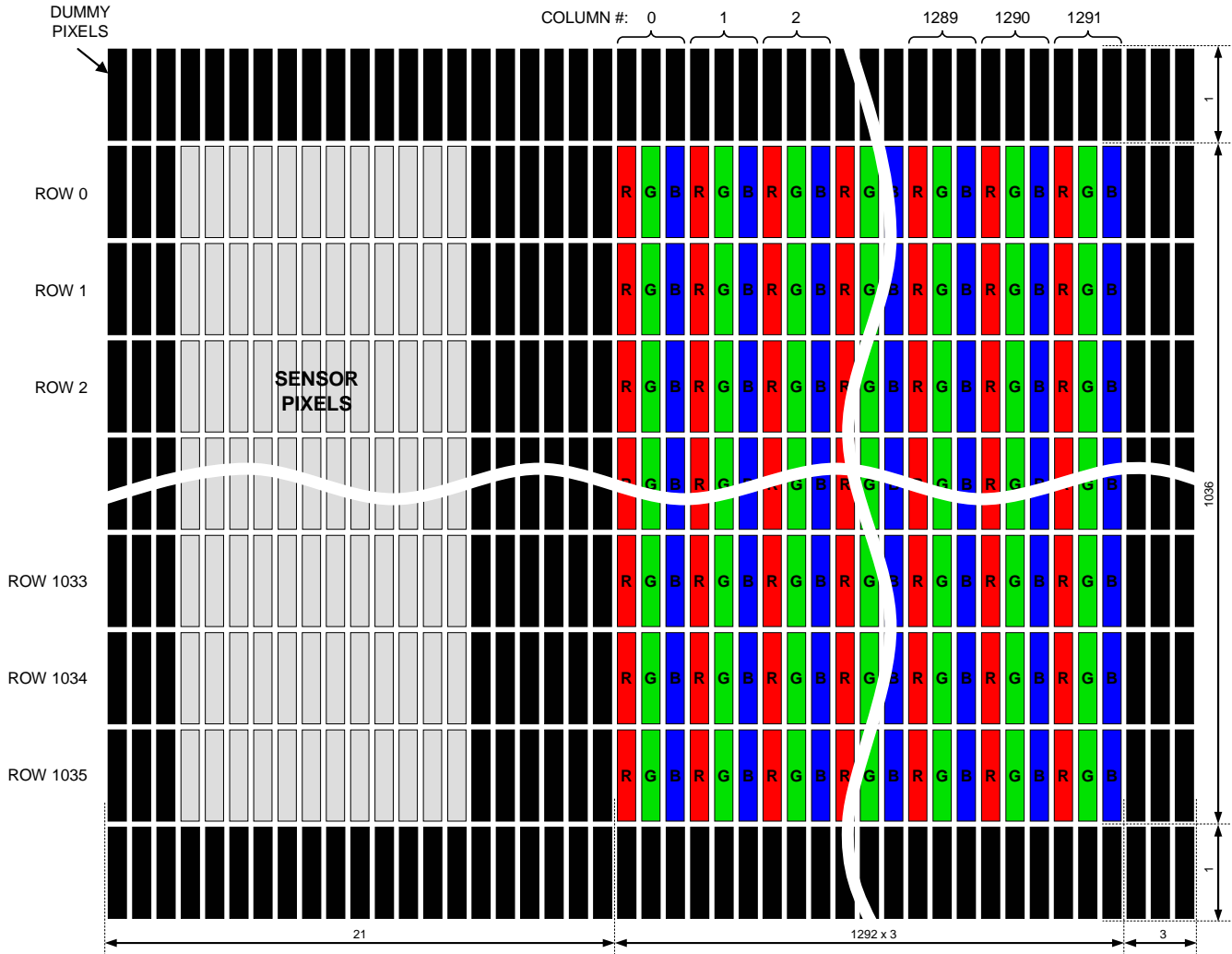
Miniature 50 pin header connector part number: Hirose DF12D(3.0)-50DP-0.5V(81)

Table 4-1 : Input / Output Pin Description

6/12/2009

Pin #	Pin Name	I/O	Signal Level	Description
1	VDD2.5	IN	Power	Logic and I/O power supply (2.5V)
2	VDD5	IN	Power	Analog and Array power supply (5V)
3	SCL	IN	Digital	Clock port for the serial interface (400 KHz Max)
4	VDD5	IN	Power	Analog and Array power supply (5V)
5	SDA	IN/OUT	Digital	Data port for the serial interface
6	GND	IN	Power	Power return terminal
7	SERADD	IN	Digital	Serial Interface LSB address bit. Must be connected. (2.5V CMOS)
8	GND	IN	Power	Power return terminal
9	RD0	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
10	VPG	IN	Power	Negative supply for array protection (-1.5V)
11	RD1	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
12	BI	IN	Digital	Burn In Mode selection pin. Active high. Internal pull-down. (2.5V CMOS)
13	RD2	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
14	VGN	OUT	Analog	Gamma sensor feedback signal (0 to 5V/2.5V analog output)
15	RD3	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
16	GND	IN	Power	Power return terminal
17	RD4	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
18	VSYNC	IN	Digital	Vertical Sync logic input. (2.5V CMOS)
19	RD5	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
20	HSYNC	IN	Digital	Horizontal Sync logic input. (2.5V CMOS)
21	RD6	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
22	DE	IN	Digital	Data Enable logic input used with loading RGB data. (2.5V CMOS)
23	RD7	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
24	GND	IN	Power	Power return terminal
25	RD8	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
26	SCLK	IN	Digital	Source clock input. (2.5V CMOS)
27	RD9	IN	Digital	Parallel 8-bit digital Red inputs. (2.5V CMOS)
28	ENABLE	IN	Digital	Enable logic input. When inactive, blocks row and column sequencers. (2.5V CMOS)
29	GND	IN	Power	Power return terminal
30	RESETB	IN	Digital	Asynchronous System Reset. Active low. Internal pull-up. (2.5V CMOS)
31	BL0	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
32	GN9	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
33	BL1	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
34	GN8	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
35	BL2	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
36	GN7	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
37	BL3	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
38	GN6	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
39	BL4	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
40	GN5	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
41	BL5	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
42	GN4	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
43	BL6	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
44	GN3	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
45	BL7	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
46	GN2	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
47	BL8	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
48	GN1	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)
49	BL9	IN	Digital	Parallel 8-bit digital Blue inputs. (2.5V CMOS)
50	GN0	IN	Digital	Parallel 8-bit digital Green inputs. (2.5V CMOS)

5. PIXEL ARRAY LAYOUT



6. ELECTRICAL CHARACTERISTICS

Table 6-1 : Absolute Maximum Ratings

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD	Front End Power Supply	-0.3		2.75	VDC
VAN	Array Power Supply	-0.3		5.5	VDC
VCOM	Common electrode bias	-6		0	VDC
VPG	Array Bias Supply	-3		0	VDC
VI	Input Voltage Range	-0.3		VDD+0.3	VDC
VO	Output Voltage Range	-0.3		VDD+0.3	VDC
PD	Power Dissipation			1	W
Tst	Storage Temperature	-55		+90	°C
Tj	Junction Temperature	-35		+125	°C
Ilu	Latch up current			+100	mA
Vesd	Electrostatic Discharge – Human Body Model			±2000	V

Stresses at or above those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the following tables is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability (except for the reverse bias condition. See below). Prolonged exposure to high temperatures will shorten the luminance half-life.

Table 6-2 : Recommended Operating Conditions

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD	Front End Power Supply	2.375	2.5	2.625	VDC
VAN	Array Power Supply	4.75	5	5.25	VDC
VCOM	Common electrode bias	-5	-2.0	0	VDC
VPG	Array Bias Supply	-3	-1.5	0	VDC
Tst	Storage Temperature	-55		+90	°C
Ta	Ambient Operating Temp.	-46	+25	+70	°C
Pdt	Power Consumption		200	500	mW

Table 6-3 : DC Characteristics

(Ta = 25°C, VDD = +2.5V, VAN = +5V, GND = 0V)

Symbol	Parameter	Min	Typ.	Max.	Unit
VDD	Front End Power Supply		2.5		V
VAN	Array Power Supply		5		V
VCOM	Common electrode bias	-5	-2.0	0	V
VPG	Array Bias Supply		-1.5		V
Vil	Digital input low level	GND-0.3		1	V
Vih	Digital input high level	1.8		VDD+0.3	V
Vol	Digital output low level			0.5	V
Voh	Digital output high level	2.4			V
Vsl	Hsync, Vsync input low	GND-0.3		1	V
Vsh	Hsync, Vsync input high	1.8		VDD+0.3	V
VGN	Gamma feedback signal	0		5	V
	Variability	4	30	50	%
Ipix	Average Pixel Current per frame	0	6	15	nA
Ipix_inl	Average Pixel Current Integral Non Linearity			5	%
Ipix_dnl	Average Pixel Current Differential Non Linearity			1	%

Table 6-4 : AC Characteristics

(-35°C < Ta < +70°C, GND = 0V, VDD = +2.5V, VAN = +5.0V, VCOM = -2V, VPG = -1.5V, Ipix_avg = 6 nA)

Symbol	Parameter	Min	Typ.	Max.	Unit
SCLK	Video Clock Frequency	12	-	135	MHz
CLK_Duty	SCLK duty cycle	40		60	%
Fhs	Horizontal Sync frequency	15.734		80	KHz
Fvs	Vertical Sync Frequency	30		85	Hz
Tlo	Line Overscan (% of line time)	3			%
Tfb	Frame Blanking (% of frame time)	1			%
Trst	Reset Pulse Width	100		-	µs
Cin	Digital Pins Input Capacitance		3		pF
Cvpg	Pin VPG Input Capacitance		13.6		nF
Pd VAN	Average Van Power Consumption (SXGA Mode 60 Hz refresh rate)		160		mW
Pd VDD	Average VDD Power Consumption (SXGA Mode 60 Hz refresh rate)		35		mW
Pd VPG	Average VPG Power Consumption			1	mW
Pd PDWN	Total Power Consumption in PDWN (sleep) mode*		2.5		mW
Ta	Ambient Operating Temperature	-46		+70	°C

*Note: Input data, sync and clock lines must be inactive and held low

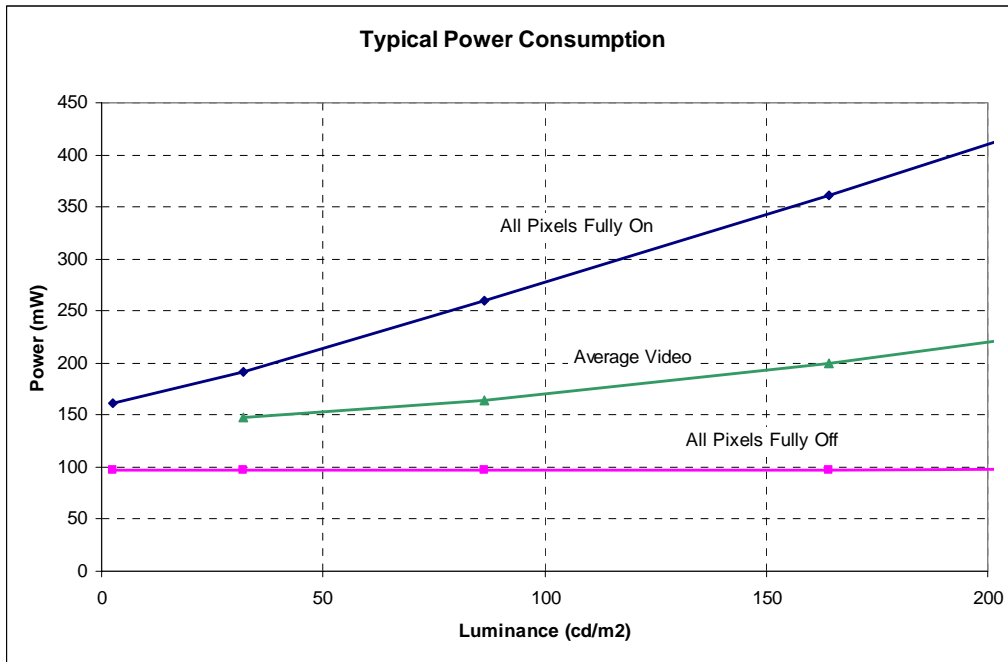
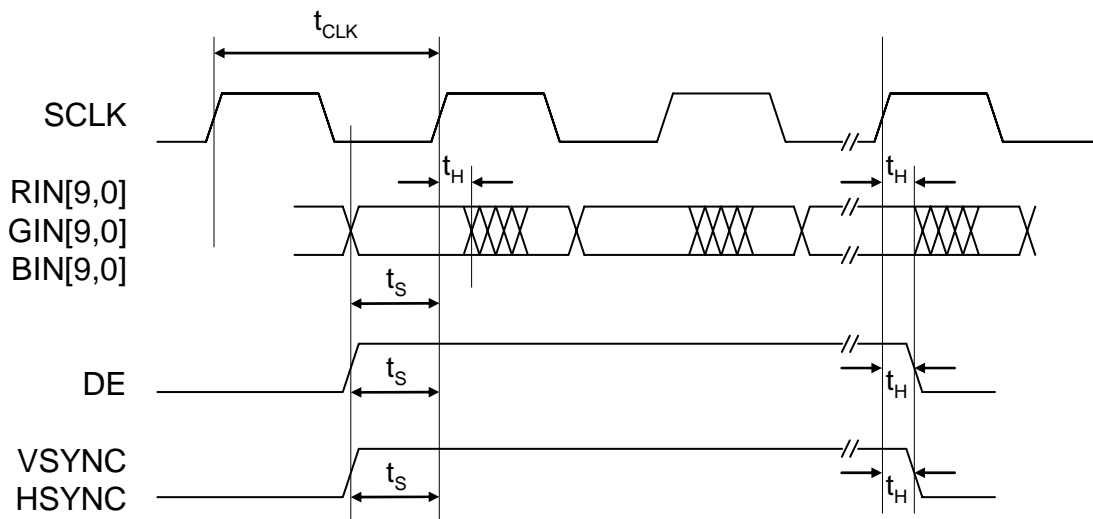


Figure 2 : Total power consumption vs. luminance at 20°C – Color SXGA

6.1 Timing Characteristics

6.1.1 Interface Timing Diagrams



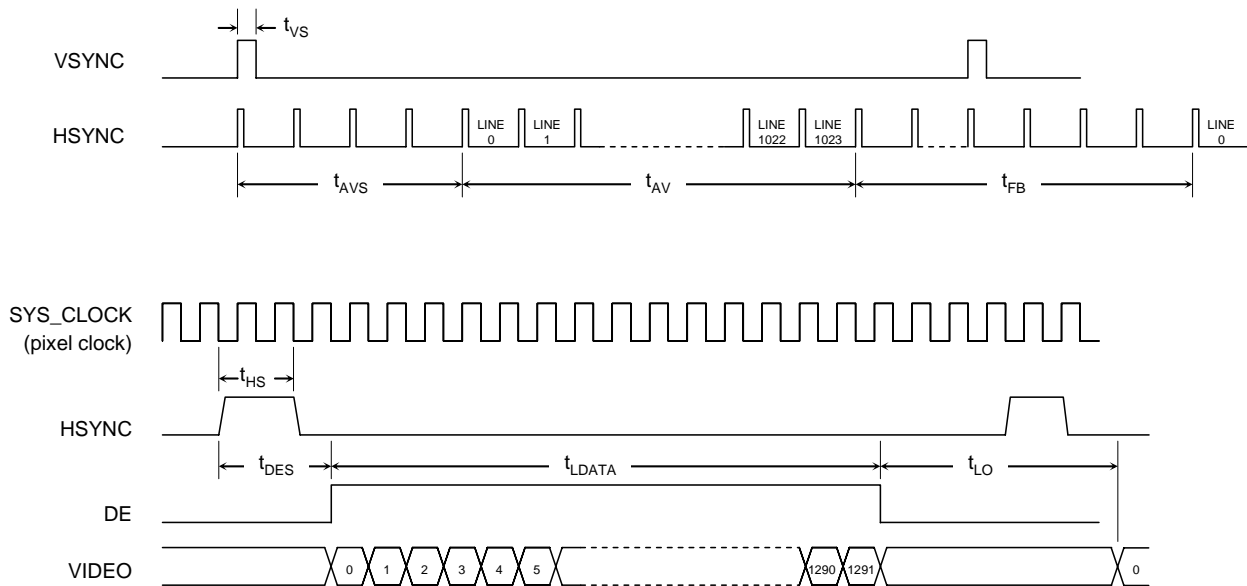
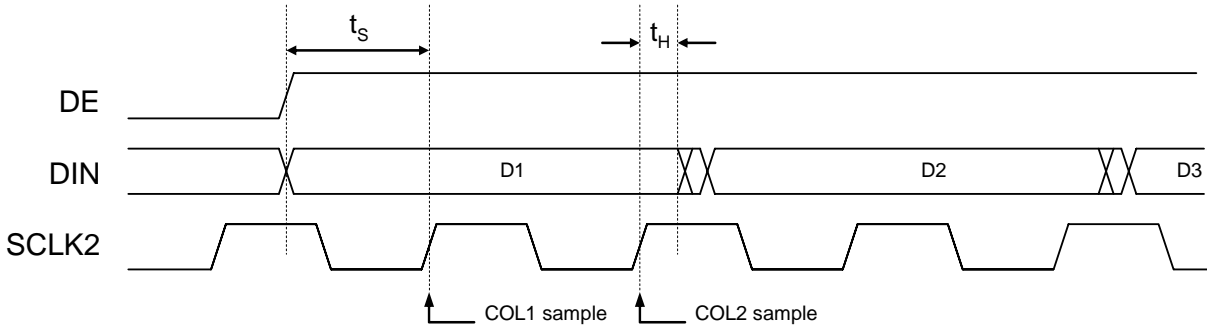


Table 6-5 : Input Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Video Input Setup/Hold (RIN/GIN/BIN)	t_s	4			ns
	t_H	1			ns
Control Signals Setup/Hold (DE/HSYNC/VSYNC)	t_s	4			ns
	t_H	1			ns
Clock Frequency	f_{CLK}		108 ¹		MHz
Clock Period	t_{CLK}		9.26		ns
Clock Duty	D_{CLK}	40		60	%
VSYNC Pulse Width	t_{VS}	1			Hsync period
Time to Active Video Start	t_{AVS}	4			Hsync period
Frame Blanking (% of frame time)	t_{FB}	1			%
HSYNC Pulse Width	t_{HS}	4			SCLK period
Time to DE Start	t_{DES}	12			SCLK period
Line Overscan (% of line time)	t_{LO}	3			%

Note 1: SXGA @ 60Hz frame rate

6.1.2 DVGA Mode Timing Diagram



6.1.3 Gamma Sensor Timing Diagram

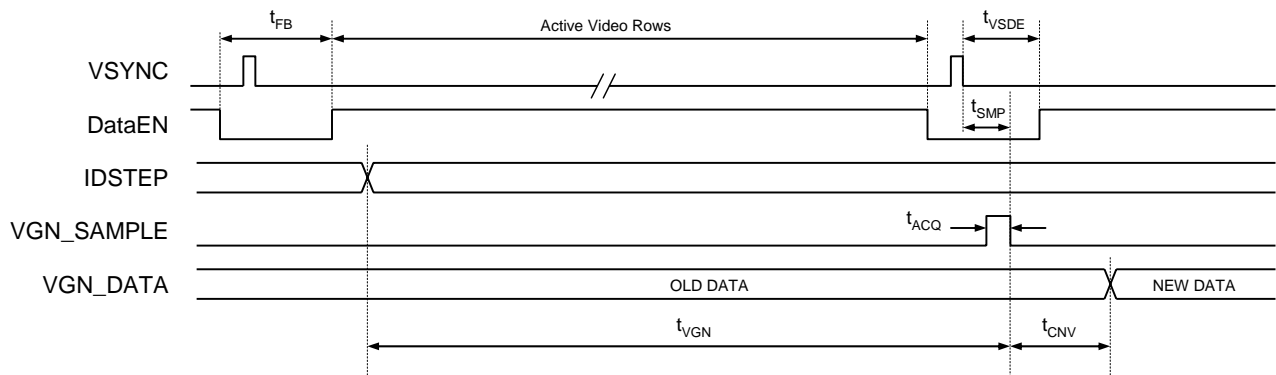


Table 6-6 : Gamma Sensor Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
IDSTEP to VGN Settling Time	t_{VGN}	10			ms
Frame Blanking (% of Frame Time)	t_{FB}	1			%
VGN Sampling Time	t_{SMP}	t_{ACQ}		t_{VSDE}	
A/D Acquisition Time	t_{ACQ}	20			μ s
A/D Conversion Time	t_{CNV}				

7. OPTICAL CHARACTERISTICS

NOTE: Every SXGA Microdisplay undergoes a 24-hour burn-in prior to ship. The characteristics documented below apply to post burn-in conditions.

Table 7-1 : SXGA XL Color Microdisplay Optical Characteristics

Conditions: Ta = +20°C, VDD = +2.5V, VAN = +5V, VPG = -1.5V, VCOM = internally generated

Symbol	Parameter	Min.	Typ.	Max.	Unit
LMAX	Front Luminance @ max gray level	0.35	140	400	cd/m ²
	Variability	0	10	22	%
CR	White to Black Contrast Ratio	1,000:1			
CIE White	CIE-X	0.270	0.300	0.340	
	CIE-Y	0.320	0.360	0.380	
CIE Red	CIE-X	0.570	0.620	-	
	CIE-Y	0.290	0.340	0.360	
CIE Green	CIE-X	0.210	0.260	0.305	
	CIE-Y	0.460	0.510	-	
CIE Blue	CIE-X	-	0.141	0.190	
	CIE-Y	-	0.117	0.170	
GL	Gray Levels Per Color	256		1024	levels
F _R	Refresh Rate	30		85	Hz
FF	Emissive Area/Total Sub-pixel Area		0.69		
U _{LA}	End to end large-area uniformity	85 ⁽¹⁾			%
S _{VH}	Pixel spatial noise at ½ luminance (1STD)			5	%
S _{LOT}	Peak-to-peak luminance variation over operating temperature range			8 ⁽²⁾	%
T _{ON}	Time to recognizable image after application of power			0.5	sec

Note 1: At 100% of gray level brightness and 80 cd/m² luminance. Luminance uniformity measured between the nominal values of five 1000 pixel zones located in the four extreme corners and the center zone of the display.

Note 2: With firmware providing temperature control of DAOFFSET setting

Table 7-2 : SXGA XL Monochrome White Microdisplay Optical Characteristics

Conditions: Ta = +20°C, VDD = +2.5V, VAN = +5V, VPG = -1.5V, VCOM = internally generated

Symbol	Parameter	Min.	Typ.	Max.	Unit
LMAX	Front Luminance @ max gray level over dimming range (IDRF, DIMCTL)	1 ⁽¹⁾	900	1800	cd/m ²
	Variability	0	10	22	%
CR	White to Black Contrast Ratio	1,000:1			
CIE White	CIE-X	0.27	0.32	0.37	
	CIE-Y	0.32	0.34	0.38	
GL	Gray Levels Per Color	256		1024	levels
F _R	Refresh Rate	30		85	Hz
FF	Emissive Area/Total Sub-pixel Area		0.69		
U _{LA}	End to end large-area uniformity	85 ⁽²⁾			%
S _{VH}	Pixel spatial noise at ½ luminance (1STD)			5	%
S _{LOT}	Peak-to-peak luminance variation over operating temperature range ⁽³⁾			8	%
T _{ON}	Time to recognizable image after application of power			0.5	sec

Note 1: Reduced operating luminance possible with additional firmware control

Note 2: At 100% of gray level brightness and 80 cd/m² luminance. Luminance uniformity measured between the nominal values of five 1000 pixel zones located in the four extreme corners and the center zone of the display.

Note 3: With firmware providing temperature control of DAOFFSET setting

Table 7-3 : SXGA XL Monochrome Green Microdisplay Optical Characteristics

Conditions: Ta = +20°C, VDD = +2.5V, VAN = +5V, VPG = -1.5V, VCOM = internally generated

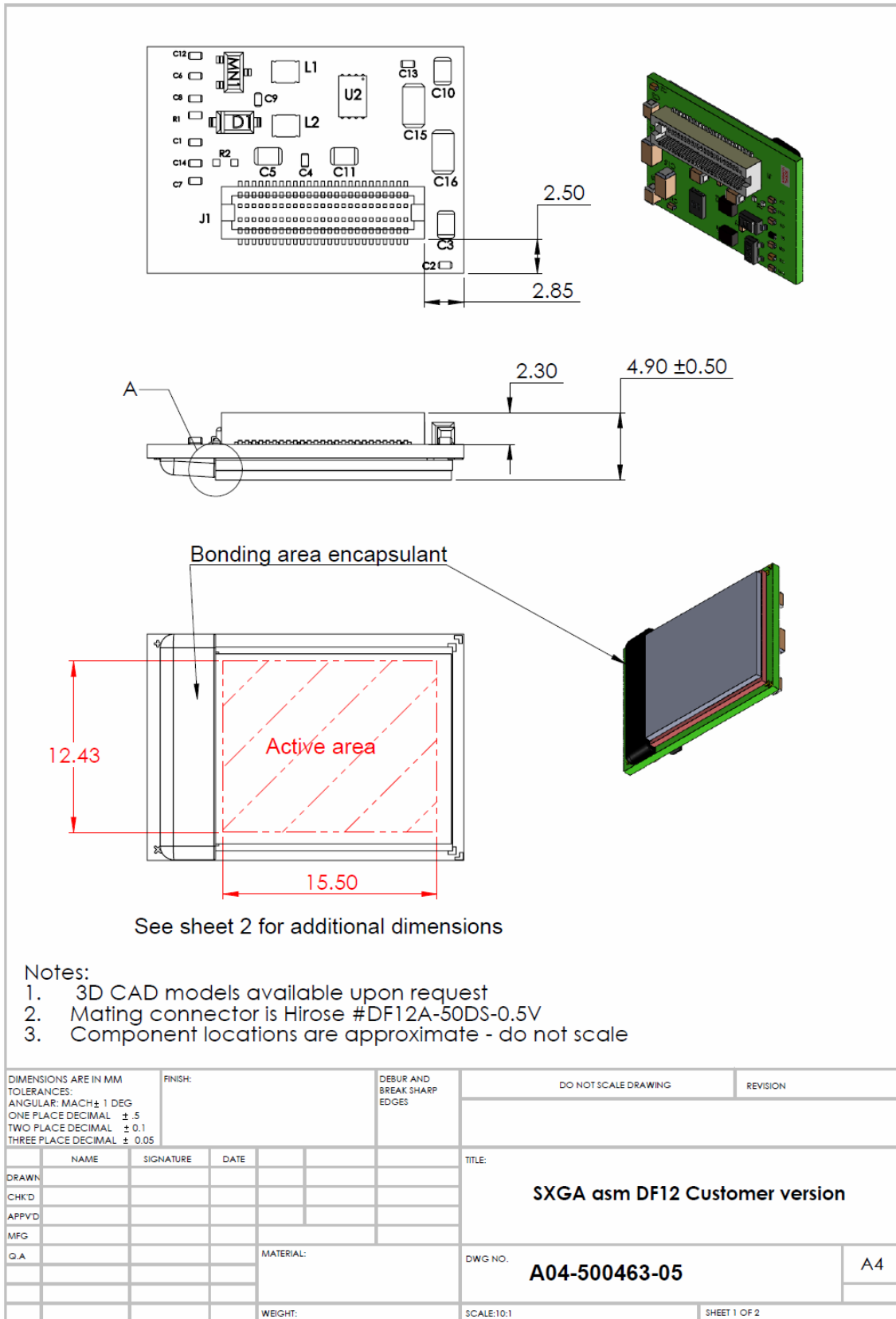
Symbol	Parameter	Min.	Typ.	Max.	Unit
LMAX	Front Luminance @ max gray level over dimming range (IDRF, DIMCTL)	1 ⁽¹⁾	1500	3000	cd/m ²
	Variability	0	10	22	%
CR	White to Black Contrast Ratio	1,000:1			
CIE	CIE-X	0.20	0.23	0.30	
	CIE-Y	0.50	0.55	0.66	
GL	Gray Levels Per Color	256		1024	levels
F _R	Refresh Rate	30		85	Hz
FF	Emissive Area/Total Sub-pixel Area		0.69		
U _{LA}	End to end large-area uniformity	85 ⁽²⁾			%
S _{VH}	Pixel spatial noise at ½ luminance (1STD)			5	%
S _{LOT}	Peak-to-peak luminance variation over operating temperature range ⁽³⁾			8	%
T _{ON}	Time to recognizable image after application of power			0.5	sec

Note 1: Reduced operating luminance possible with additional firmware control

Note 2: At 100% of gray level brightness and 80 cd/m² luminance. Luminance uniformity measured between the nominal values of five 1000 pixel zones located in the four extreme corners and the center zone of the display.

Note 3: With firmware providing temperature control of DAOFFSET setting

Mechanical characteristics



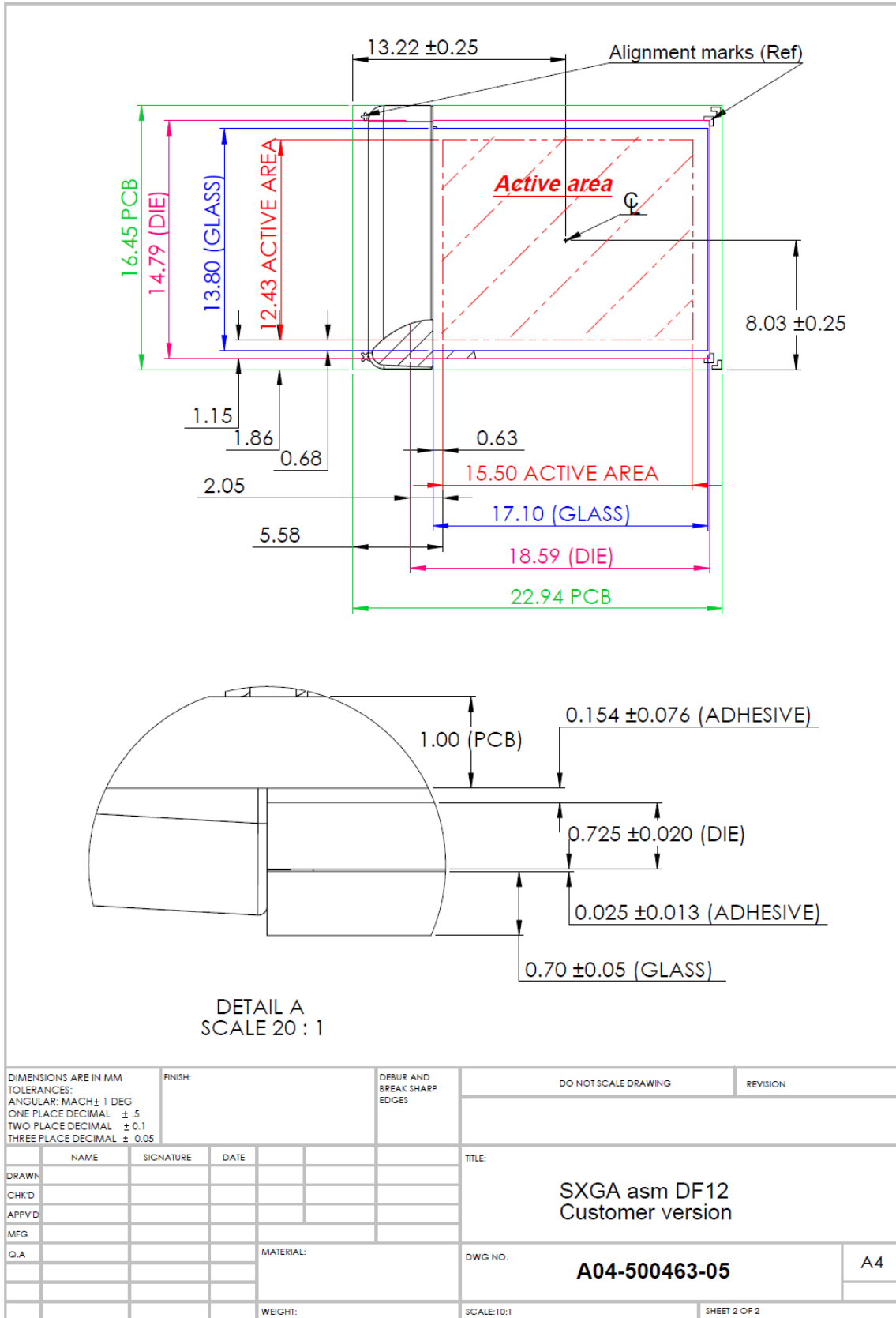


Figure 3: SXGA Assembly Drawing with 0.7mm Glass Cover (A04-500463-05)

Connector J1

Manufacturer: Hirose
Manufacturer Part Number: DF12D(3.0)-50DP-0.5V(81)

Mating Connector Information

Manufacturer: Hirose
Manufacturer Part Number: DF12A(3.0)-50DS-0.5V(81)

Weight: < 2.5 grams

Printed Circuit Board Material: FR4
Printed Circuit Board Tolerances: ± 0.3 mm (both axes)

Flame Resistance Information

- Printed Circuit Board UL94V-O
- Connector UL94V-O
- Wirebond Encapsulant Flammability: 1 Flash point: 93°C
- Cover Glass Non flammable
- Silicon IC Non flammable

8. CLEANING HANDLING AND STORAGE RECOMMENDATIONS

8.1 Cleaning

When cleaning the displays we recommend the use of TECH-SPEC lens cleaner, manufactured by Edmund Optics Inc. and Alpha wipes 1010

The use of diluted IPA is also approved for cleaning the display. Care must be taken to ensure no residue remains after wiping the display surface

8.2 General handling considerations

- Do not expose the display to strong acids, bases, or solvents.
- Do not expose the display surface to UV or other strong ionizing radiation
- Temperatures in excess of the specified operating and storage range can cause irreversible damage to the display.
- Do not allow sharp objects to contact the exposed regions of the silicon display chip.
- Avoid immersion of the display in any liquid.
- The glass cover slip protects the display surface from most forms of damage and may be cleaned using techniques appropriate for fine lenses.
- Avoid applying force to the glass relative to the display chip in compressive, tensile, and shear directions.



Figure 4: Best method of handling the displays



Figure 5: Avoid this method of display handling

8.3 Static Charge Prevention

The microdisplay is sensitive to electro-static discharge damage. The following measures are recommended to minimize ESD occurrences:

- When handling the microdisplay, operated under a flow of ionized air to discharge the panel
- Use a conductive wrist strap connected to earth ground via a 10 M-Ohm resistor.

- Wear non-chargeable clothes
- Keep stored displays away from charged materials

8.4 Protection from Dust and Dirt

It is also recommended that all display handling operations take place in a clean environment. The use of ionized nitrogen gas is the preferred method of removing particles from the surface.

8.5 Short Term Storage

For short term storage (one to two weeks or less), the displays should be kept in their original container at room ambient and the typical controlled office environment.

8.6 Long Term Storage

For displays that will be stored for a longer period (a few weeks and up), it is recommended to keep displays stored in a dry environment near or at room ambient (20°C typically) whenever possible prior to installation into an optical subsystem.

There are several ways to achieve this:

- Dry storage cabinet
- Dry Nitrogen cabinet
- Nitrogen sealed bag
- Vacuum sealed bag with desiccant

8.7 System Integration

Care must be taken when attaching the SXGA microdisplay to a housing. Specifically, there should be no contact between the top of the silicon die and any surface: the glass cover is the only approved surface that can be in contact with a housing cover on the front side of the microdisplay. The rear side of the circuit board assembly (where the connector is) can be used with adhesives to attach to a frame or housing.

The use of Super-X adhesive to attach the SXGA microdisplay to a frame or housing is approved.

9. DETAILED FUNCTIONAL DESCRIPTION

9.1 Video Input Interface

The 30-bit digital input port is comprised of three 10-bit data busses that make up the RGB data inputs. Separate synchronization signals (VSYNC and HSYNC) and the pixel clock (SCLK) are to be provided by the external video source. The data valid signal (DE) is used to signal the start of loading a row of data into the internal line memory. An active ENABLE signal is required for the Stereovision mode (inactive for all other modes, except Interlaced Video). The timing diagram for the input data bus is shown in Figure 6.

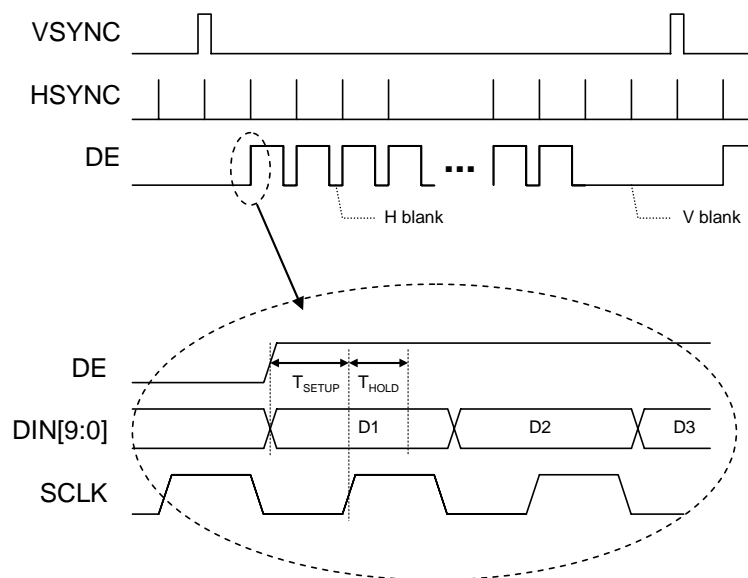


Figure 6 : Input Data timing diagram.

The input data to the display requires certain formatting that must be applied by the external drive electronics as described below.

9.1.1 Gamma Correction

Due to the non-linear electro-optic characteristic of the OLED pixel, a gamma correction signal must be applied to the video input signal to achieve a linear system response for the display. Since the optimum gamma curve will vary with temperature and luminance, it should also be regularly updated to account for changes in operating conditions. The color balance for the display can be modified by controlling the gamma individually for each of the three color data channels. Figure 7 illustrates the behavior of different components of the SXGA display system. The OLED response curve shown in the figure is an example

of the typical optical response to input data of the microdisplay and demonstrates its highly nonlinear characteristic. The Gamma Correction function shown in the figure is obtained by inverting the OLED response function. As demonstrated by the measured system response curve in the figure, the overall system display response becomes linear when the source video data is modified by the Gamma Correction function before being applied to the SXGA.

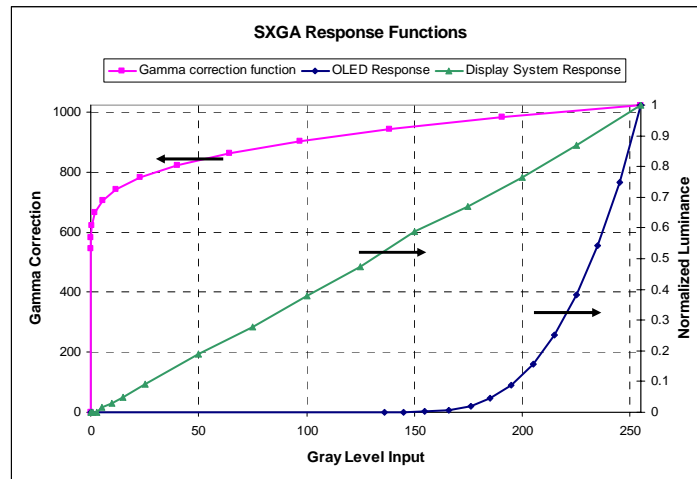


Figure 7: Gamma corrected system response characteristic

As shown in Figure 8, a typical SXGA application will include a 256x10-bit look-up-table for each color channel located in the data path between the video source and the display. The LUT, which is contained in an external FPGA, converts the 8-bit data byte for each color of the video source into a 10-bit output data word for driving the microdisplay. The LUT is programmed with the gamma correction function required to linearize the system for the current operating conditions. Due to the non-linear characteristic of the OLED display, a 10-bit input to the SXGA is used to ensure a linear 8-bit optical response with better than 1-lsb accuracy. The LUT data must be in Gray Code format as described in section 9.1.2.

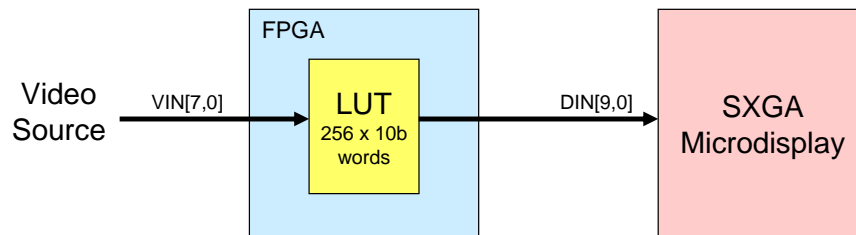


Figure 8: Gamma correction using a look-up-table (LUT)

On-chip support for generating the gamma correction function in the form of an 8-segment piecewise-linear function is described in section 9.4.5. A total of 8 data points (Q1...Q8) that lie on the gamma curve as shown in Figure 9 are provided by the display chip while point Q0 is a fixed value set by the

user. The external microcontroller can use this information to generate intermediate data points for the entire 256 point curve by linear interpolation.

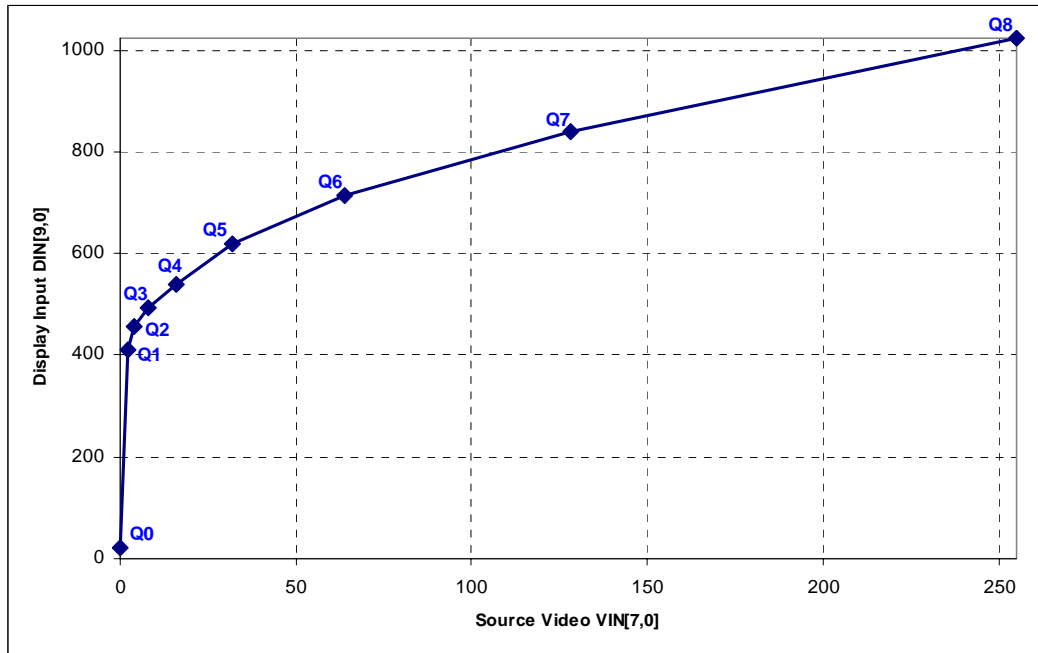


Figure 9: Typical SXGA gamma correction function

9.1.2 Gray Code Format

Input data to the SXGA digital port must be in Gray Code format to match the gray-code global counter used in the display chip. The conversion is carried out on each 10-bit color vector by the external drive electronics according to the following relationships:

$$\begin{aligned}
 G[0] &= B[0] \text{ XOR } B[1] \\
 G[1] &= B[1] \text{ XOR } B[2] \\
 G[2] &= B[2] \text{ XOR } B[3] \\
 G[3] &= B[3] \text{ XOR } B[4] \\
 G[4] &= B[4] \text{ XOR } B[5] \\
 G[5] &= B[5] \text{ XOR } B[6] \\
 G[6] &= B[6] \text{ XOR } B[7] \\
 G[7] &= B[7] \text{ XOR } B[8] \\
 G[8] &= B[8] \text{ XOR } B[9] \\
 G[9] &= B[9]
 \end{aligned}$$

where G[9,0] is the 10-bit Gray word corresponding to the 10-bit binary word B[9,0].

9.1.3 Row Data Expansion

Since the display is comprised of 1292 column lines, the external drive electronics should add 12 dummy pixels with black data to each row of 1280 pixels provided by the source signal. The dummy pixels can be distributed between the start and end of the row data according to the desired horizontal location of the active window within the pixel array.

9.2 D/A Conversion

In this design the conversion of the video input signal into an analog drive signal at the pixel is carried out in a two step process during each horizontal clock period. The digital input video data is first transformed into a precise time delay based on counts of the global RAMP clock. Second, the time delay triggers the column switch to sample the voltage of a linear ramp and to store the analog value on the column line capacitor. The selected pixel circuit copies the analog data and uses it for driving the OLED diode until it is refreshed during the next frame period.

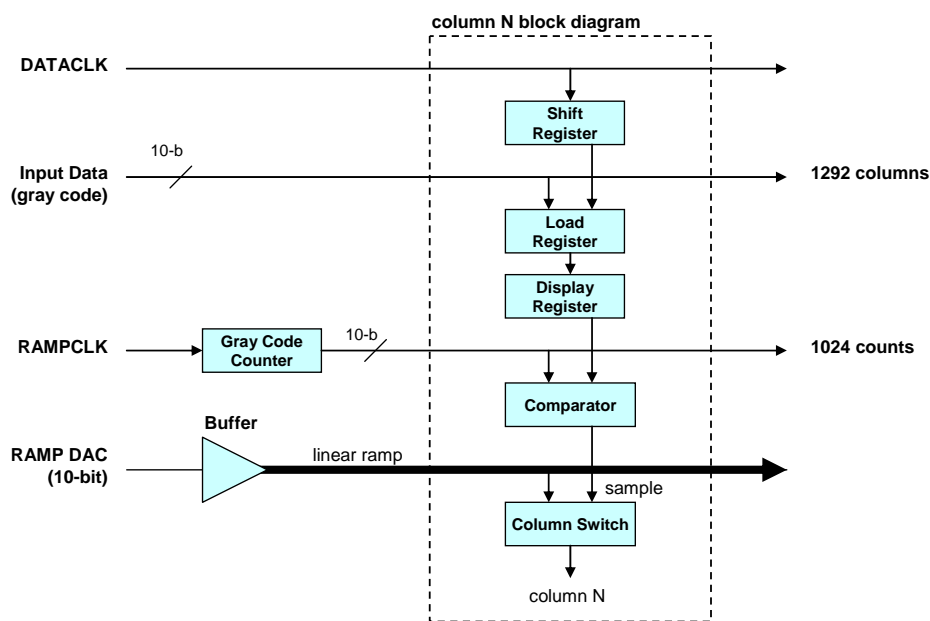


Figure 10 : Data sampling for Column N

A block diagram of one column drive circuit is shown in Figure 10. The 1292 Display registers form a line memory that facilitates a pipeline mode of operation in which video data is converted to analog form and sampled by the pixels in row M during the same line period that video data for row M+1 is loading into the LOAD registers. At the end of each line period the data in the LOAD registers is transferred in parallel into the DISPLAY line memory. The externally supplied SCLK clock is used for both loading input data into the chip and for advancing the global column counter. There is a maximum latency of 2 line periods before data is displayed.

A timing diagram for the data sampling process is shown in Figure 11. The internal Ramp Generator operates at the HSYNC frequency and outputs a linear ramp with a slow rise-time and a fast reset capability that is buffered and applied to all the pixel array columns simultaneously. The RAMP signal starts synchronously with HSYNC (after a delay) with a positive slope from a zero voltage level and rises to a voltage near the VAN rail after 1024 SCLK clock cycles as determined by a 10-bit counter. The start position of the RAMP can be adjusted via register bits RAMPDLY1 and RAMPDLY2, its peak value can be set using register DAOFFSET, and the duration of the flyback transition can be selected between two options by the FLYBTIME bit in register RAMPCTL.

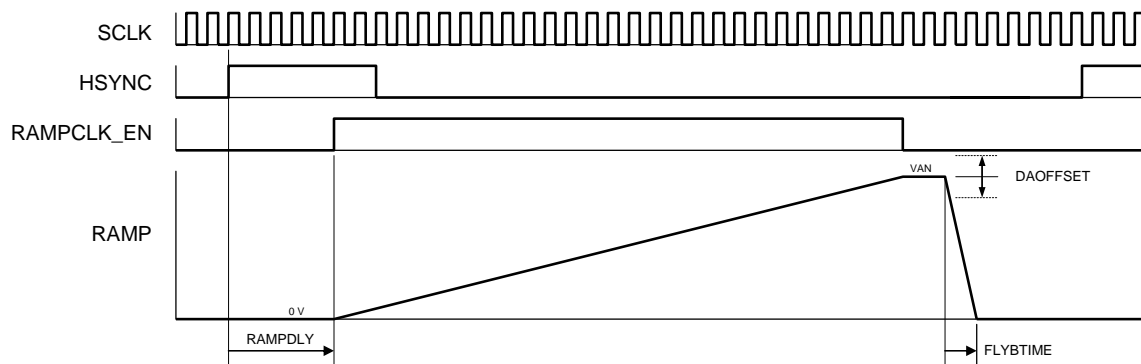


Figure 11 : Timing diagram for column data sampling

9.3 Format and Timing Control

Various control signals for the horizontal and vertical sequencers that are needed to implement the specified video formats are generated in the Timing & Control Logic block. The specific timing parameters are set by registers VINMODE, DISPMODE, TOPPOS, and BOTPOS using the serial interface.

The display starts up with the array in the off-state (black) by default and requires a command to the DISPOFF register bit via the serial interface to turn the display on. This provides the user with an opportunity to change the default startup conditions before the display lights up.

Bi-directional scanning is supported in both orientations via the DISPMODE register. Bit VSCAN sets the vertical scan direction, and bit HSCAN sets the horizontal scan direction.

Selection among the main supported display formats is done via register bits RESOLUTION, TOPPOS, BOTPOS, and the external drive electronics. Bit RESOLUTION in the DISPMODE register is used to set the counter that defines the number of active video rows to be either 1024 (default), 720 or 960 (line doubled). For resolutions lower than the native resolution the inactive rows are driven to black. In the 960 mode (DVGA), used for VGA input format only, both the line doubling feature, where each line of data drives a row-pair, and the pixel-doubling feature, where each pixel is written into a column-pair resulting

in 1280 visible pixels, are activated. In DVGA mode the SCLK provided by the drive electronics must run at double the frequency of the video source clock for pixel doubling to be achieved.

The starting row is determined by register TOPPOS and the ending row by register BOTPOS, which are set by default so the active window in SXGA mode is vertically centered in the array. These registers allow the active window to be shifted vertically in 1 line steps by up to ± 6 lines in the SXGA mode and up to ± 255 lines in HD720 mode. In DVGA mode the active window can be shifted in 2 line steps by up to ± 38 lines.

The starting column is determined by the external drive electronics which must add 12 dummy black pixels to each row of incoming data as described previously. This allows the active window to be horizontally shifted in 1 pixel steps by up to 12 pixels total.

9.3.1 Interlaced Mode

Bit SCMODE in the DISPMODE register is used to select either progressive or interlaced mode for all formats. By default (SCMODE=0) the normal progressive mode is active. Interlaced modes are limited to a maximum of 512 and a minimum of 240 active rows per field. In the case of interlaced VGA format, automatic line doubling is activated in which the shift register drives sequential pairs of rows. Figure 12 shows the interlace option for VGA with row doubling.

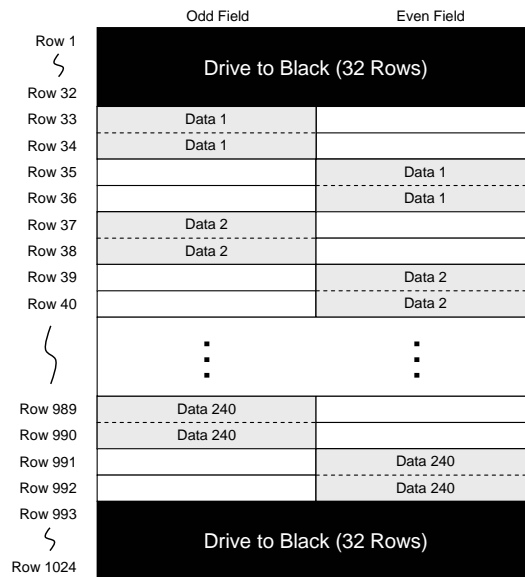


Figure 12 : Interlace option showing VGA mode with line doubling

Field status in interlaced mode is provided via the ENABLE input pin. The state of this pin is latched on the falling edge of VSYNC. When register bit SET_FIELD = "0" then a logic low at the ENABLE pin indicates that Field 1 (odd field) is active, and a logic high indicates that Field 2 (even field) is active. The opposite states are indicated when SET_FIELD is set to 1.

9.3.2 Stereovision

The SXGA is designed with binocular stereovision applications in mind. As a result of the fast OLED response time and the presence of a storage capacitor at each pixel, the microdisplay can operate at low refresh rates without showing flicker.

This will allow the displays to be used with a frame or field sequential (more generally know as time sequential) stereovision mode using a single video input channel, and therefore providing a simple means to leverage the capabilities of PC compatible computers using stereo compatible graphics adapters, such as the Nvidia GeForce series. The frame sequential stereovision mode supported should follow the Video Electronics Standards Association (VESA) Connector and Signal Standards for Stereoscopic Display Hardware. This standard is available from VESA at www.vesa.org.

The ENABLE input pin will allow for a direct implementation of the VESA standard without additional external components. The microdisplay can be programmed for either an active high or low Enable, allowing a single signal to be used with two displays. In such a configuration, one display scans and displays while the other one holds and displays.

The ENABLE input acts, when set low, as a mask for HSYNC and VSYNC. It does not blank the display but prevents it from acquiring another frame of data until released. This is a real time input. The active state (high or low logic level) is programmed by the SET_ENABLE bit in the VINMODE register.

The 3D-MODE bit of the DISPMODE register will be used to set either the Stereovision mode of operation (1) or Normal (non-3D) operation (0).

Frame Sequential Mode:

In Time Sequential Mode each video frame contains information for either the left or right eye. When 3D-MODE="1" the SCMODE bit in the DISPMODE register is set to Progressive Scan Mode (00H) for frame sequential mode. The following description for Frame Sequential operation assumes the source is in compliance with the VESA standard mentioned above, where the data for the left eye is provided while the Enable signal is at the logic high level, and the data for the right eye display is provided while the Enable signal is at the logic low level. The stereovision mode is controlled by both the Enable input pin and by the SET_ENABLE bit of the VINMODE register. The Enable input signal is sampled into the circuit by a flip-flop clocked on the falling edge of VSYNC and the sampled value will be used for the next frame. (The Enable signal is generated by the graphics software and may not be synchronized to the VSYNC signal).

To activate the stereovision mode, the right eye display needs to be configured with Enable active low (SET_ENABLE="0"). This will allow the right eye microdisplay to hold the previous frame while the Enable input is high. The left eye display must be configured with Enable active high (SET_ENABLE="1"). Thus the two Enable inputs can be tied together to the incoming Stereo Sync

signal provided by the graphics adapter (or other custom source). This is illustrated by the timing diagram shown in Figure 13.

Line Interleaved Mode:

In Line Interleaved Mode each video frame contains information for both the left and right eyes. Consequently, the resolution is reduced in half for each display but they both run at the full frame rate. The operation of the Enable input pin and the SET_ENABLE bit will be similar to Frame Sequential Mode except that now the Enable input toggles at the line rate.

For non-3D-Mode operation, the SET_ENABLE bit can be set to either 0 (logic low) or 1 (logic high), and the Enable pin input needs to be tied to VDD (2.5V).

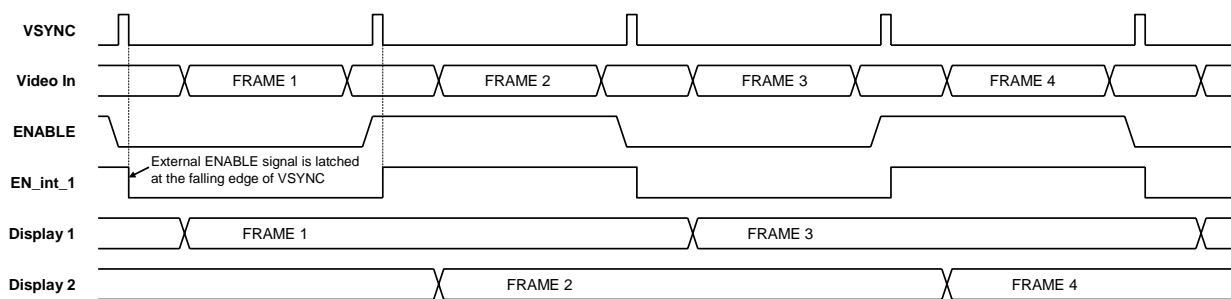


Figure 13 : Timing for frame sequential stereovision mode

9.4 Sensor Functions

9.4.1 Temperature Readout

An on-chip temperature sensor provides continuous device temperature information via the serial interface. The sensing circuitry allows for calibration at power-up via dedicated registers, TREFDIV[5,0] and TEMPOFF[7,0]. The temperature reading is digitized on-chip and stored in a dedicated register, TEMPOUT[7,0]. A register bit, TSENPD in register PWRDN, is able to power down the sensor.

The temperature sampling period is controlled by register TUPDATE[7,0] which allows the temperature reading to be updated between every 50msec to 4.25sec when operating at a 60Hz frame rate.

9.4.2 Luminance Regulation Sensor

Register VGMAX[7,0] controls the pixel drive voltage used for regulating the maximum luminance value. By default this level is set to about 4.95V when the VAN supply is equal to 5V to avoid saturating the video buffers. It can be adjusted over a range of 4 to 5V.

Register DAOFFSET[7,0] is used to set the maximum value of the internal Ramp DAC generator. This value should match the internal VGMAX setting for best luminance accuracy and control. The optimum setting can be derived by measuring luminance for different values of DAOFFSET as described in 11.8.

9.4.3 Pixel Bias Sensor

Register BIASN[1,0] sets a bias current for the OLED array in order to achieve improved control of black level and color saturation at the expense of a small increase in power consumption. In the default setting (BIASN=1) the bias contributes to a 10mW increase of power consumption for the array. It is recommended to use the BIASN=2 setting for best performance.

9.4.4 Luminance Control (Dimming)

A variable luminance level is achieved by controlling the maximum pixel current while maintaining the largest possible dynamic range. Dimming control for the display is effected by adjusting the 7-bit register DIMCTL via the serial interface to provide 128 linear steps in brightness ranging from near zero to the maximum level set by register IDRf. This functionality is only available for VCOMMODE=0 or 1.

The bits IDRf_COARSE in register IDRf provide a coarse adjustment of the maximum luminance level, while the IDRf_FINE bits enable the coarse level to be fine tuned. Figure 14 shows the typical luminance output at gray level = 255 in a color display for various settings of the IDRf and DIMCTL registers.

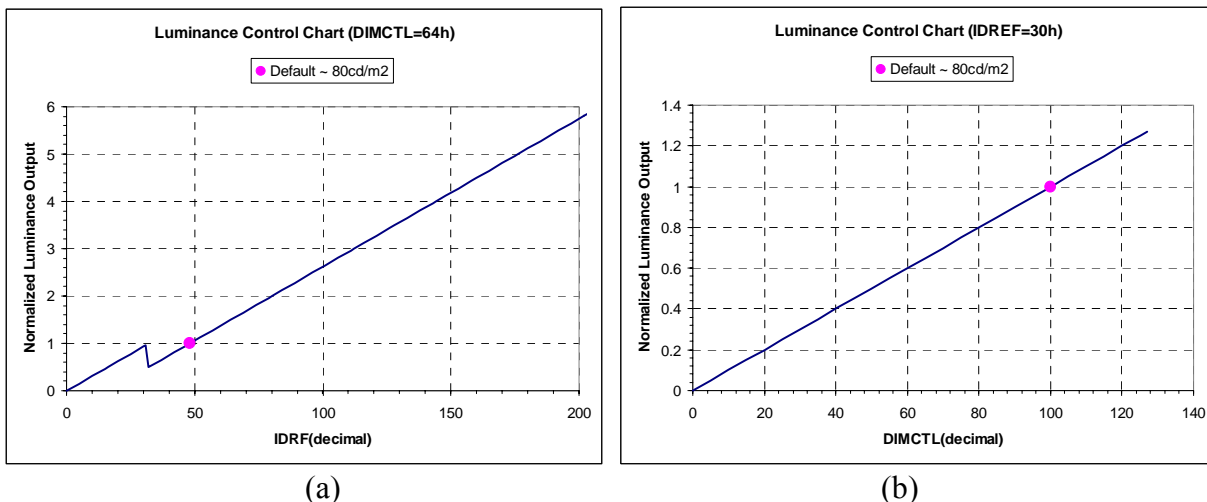


Figure 14 : Typical maximum luminance for various IDRf (a) and DIMCTL (b) settings

Large step changes in either the IDRf or DIMCTL register values are not recommended as they may result in unstable dimming control and high component stresses. The recommended procedure for increasing luminance is to increment either of the control registers by only 1h per I²C write instruction until the desired final luminance is reached. For example, to increase IDRf from 30h to 50h would require a sequence of 32 write instructions.

9.4.5 Gamma Correction Sensor

The gamma sensor is provided as an aid to generating a linear optical response from the SXGA display system. As described previously, an external 256-entry look-up-table is required to transform input video data into a gamma-corrected data signal for driving the microdisplay input port. The SXGA display generates an internal real-time representation of the gamma correction curve for the current operating conditions. This representation is in the form of an analog voltage waveform which can be sampled one point at a time at the VGN pin for eight specific values on the curve. A specific value VGN_i , corresponding to one of 8 internally fixed grayscale levels GL_i , is selected by setting bit IDSTEP in register GAMMASET via the serial port. The VGN signal can be set for a full-scale output range of either VAN (default) or VAN/2 by setting bit VGNSSEL in register GAMMASET. Eight sequential measurements are required to complete the gamma table. The gamma table can then be used to reconstruct an approximation of the ideal gamma correction curve using piece-wise linear interpolation, or by employing a curve fitting algorithm to achieve more accuracy if desired. This function is only available for VCOMMODE=00h.

An external A/D converter is required to convert each VGN measurement into digitized form and to store the values in a microcontroller for further processing. A full frame period following a change in the IDSTEP bit should be provided to allow the VGN signal to settle before sampling it to 10-bit precision by the external A/D converter. It is recommended to sample the VGN signal during the frame blanking interval for best results.

The VGN readings are normalized and converted to a 10-bit full-scale word $DVGN_i[9,0]$ using the following expression:

$$DVGN_i[9,0] = \frac{VGN_i}{VGN_{MAX}} * 1023$$

where VGN_{MAX} is either VAN or VAN/2 as determined by bit VGNSSEL. Each of these data values must be further multiplied by a correction factor CF_i to obtain the Gamma table coefficients as follows:

$$GC_i[9,0] = DVGN_i * CF_i$$

where the empirically determined values for factor CF_i are given in Table 9-1.

Table 9-1: Correction Factor values

CF1	CF2	CF3	CF4	CF5	CF6	CF7	CF8
0.880	0.909	0.929	0.953	0.973	0.987	0.992	1

Using the derived values for GC_i and their corresponding grayscale coordinates GL_i , the 8-entry Gamma Correction table consisting of data points $Q_i = (GL_i, GC_i)$ can be constructed. The outcome of a typical gamma sensor measurement and calculation procedure is shown in Table 9-2.

Table 9-2: Sample Gamma Correction Table

i	1	2	3	4	5	6	7	8
$IDSTEP[0]$	0h	1h	2h	3h	4h	5h	6h	7h
$VGN_i(volt)$	1.839	1.876	1.913	1.964	2.045	2.159	2.318	2.500
$GC_i(dec)$	662	698	727	766	814	872	941	1023
$GL_i(dec)$	2	4	8	16	32	64	128	255

The full 256-word LUT is derived from the Gamma Coefficient Table using linear interpolation to generate intermediate data points as illustrated in Figure 15. The input to the LUT for each color of the video source is represented by the 8-bit signal $VIN[7,0]$, and the output of the LUT (which is also the input to the microdisplay) is represented by the 10-bit signal $DIN[9,0]$. For example, the Y coordinate for the intermediate point $Q(x, y)$ on the line segment formed between the gamma table points Q_6 and Q_7 is obtained by:

$$Y = Y_6 + (Y_7 - Y_6) * \frac{(X - X_6)}{(X_7 - X_6)}$$

The intermediate points for other line segments are found in similar fashion. A software routine in the system microcontroller is used to perform the necessary calculations. The software is also used to convert the LUT data into Gray Code format before loading it into the data-path LUTs in the FPGA. A buffer LUT should be used in the FPGA to temporarily store the data as it is transferred from the microcontroller via the serial port. When the buffer LUT is full, the data can be rapidly transferred to the data-path LUTs during a frame blanking time to avoid disturbing the displayed image.

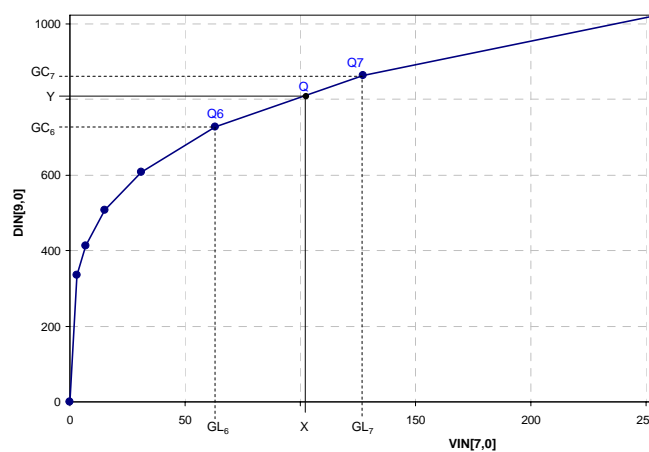


Figure 15 : Generating intermediate points by linear interpolation

A smooth transition of the gamma curve at the lowest gray levels is essential for best performance of the display at the black end of the gray scale. Refer to Figure 16 for an illustration of the recommended approach for calculating the gamma curve at low gray levels. The LUT data points for gray levels 1 to 4 can all be generated by linear extrapolation from the gamma points Q1 and Q2. The LUT data point for gray level 0 (also defined as Q0) is a fixed value that is user-defined, and normally should be set to a very low value, e.g. 1, to ensure the best black level. The value for Q0 is shown on the graphical interface screen supplied with the SXGA design reference kit for user convenience. It is not affected by the gamma sensor signal and can only be changed manually by user input.

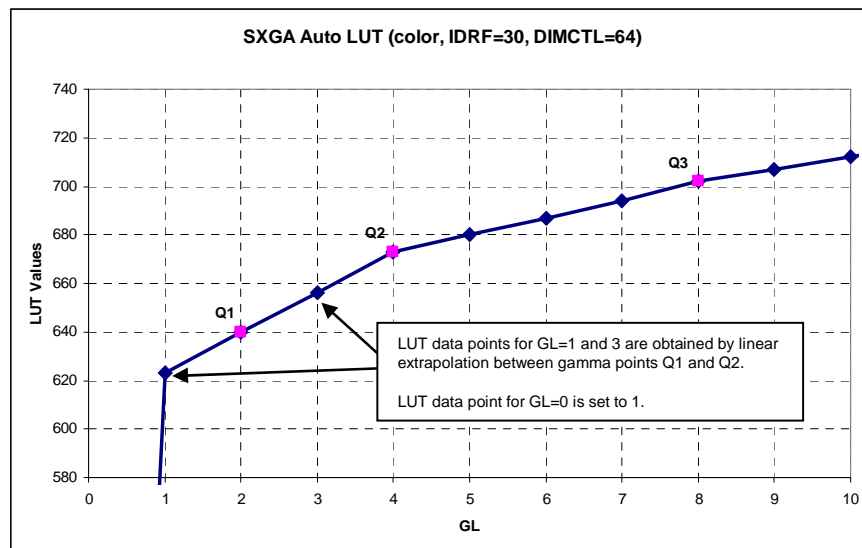


Figure 16 : Gamma curve at low gray levels

An arbitrary optical response function for the microdisplay can be obtained by performing an additional operation on the gamma coefficients before generating the gamma correction curve as described previously. For example, the relationship between the output luminance of the display (y) and the gray level input to the LUT (x) can be defined in terms of the system gamma (γ) by the following expression:

$$y = x^\gamma$$

The corresponding gamma coefficients are then given by the following expression:

$$GC_i^\gamma = \left(\frac{VGN_i}{VGN_{MAX}} * CF_i \right)^\gamma * 1023$$

For the case of a linear optical response ($\gamma=1$) this expression reduces to the simpler form given previously. Examples of gamma curves generated from the same VGN values for different settings of the

System Gamma parameter are shown in Figure 17 and the corresponding system response curves for the display are given in Figure 18.

The System Gamma function is implemented in DRK Firmware V3.3 and is accessible to the user in the DRK UI Software V1.9.

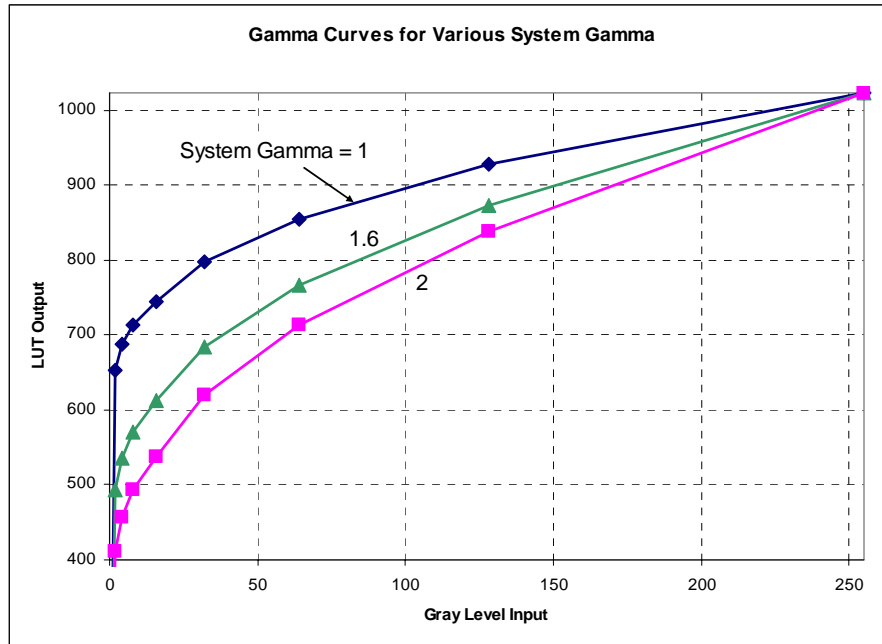


Figure 17 : Gamma curves for arbitrary System Gamma

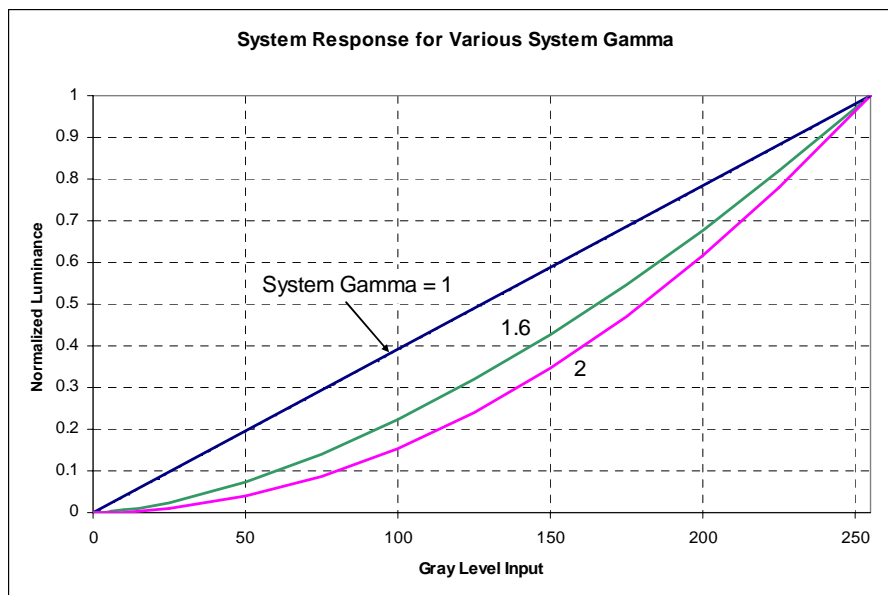


Figure 18 : Display system response for arbitrary system gamma

9.5 DC-DC Converter

An on-chip dc to dc converter controller allows for the generation of the OLED cathode supply, relying on a few external passive components assembled on the display carrier board. The converter is an adjustable inverter that converts VAN to a negative supply used to bias the OLED via the VCOM input pin. Adjustment is managed by the control logic and registers VCOM[7,0] and VCOMMODE[1,0].

The converter adjustment comes from two sources:

- A nominal value set in a dedicated register that provides for the room temperature voltage level.
- The output of an internal VCOM sensor circuit. This feature can be enabled/disabled via register setting to allow full external control (via register VCOM).

A block level schematic of the Cuk converter that is employed in the SXGA application is shown in Figure 19.

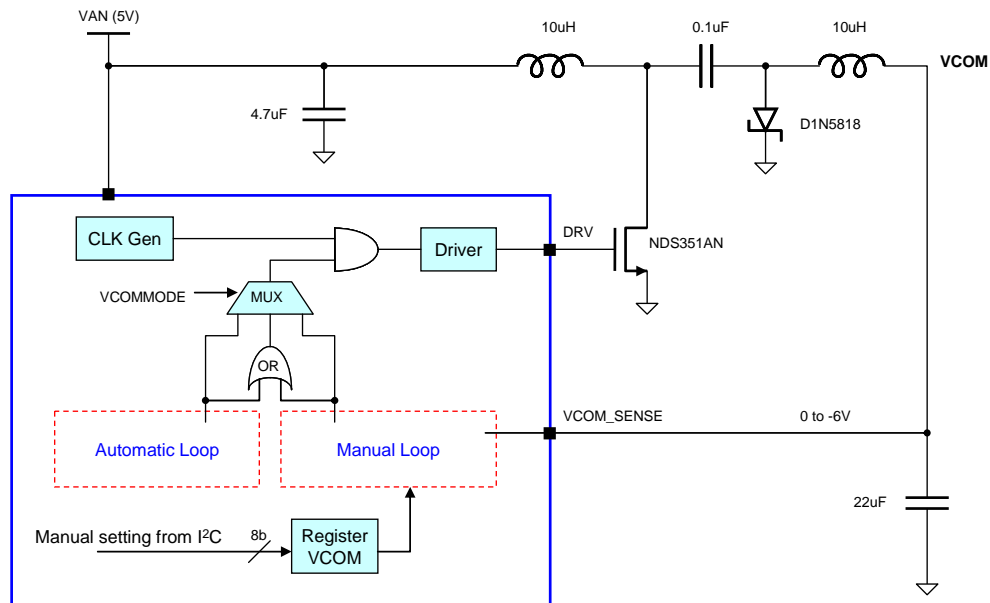


Figure 19 : Schematic of DC-DC controller function

Three modes of operation, selected via register VCOMMODE, are provided for the controller function. Mode 1, selected by default (VCOMMODE=0), activates the Automatic Loop which provides VCOM regulation based on an internal current feedback sensor. In this mode the cathode supply is automatically regulated in order to maintain a constant maximum OLED array current over changes in temperature and luminance. The cathode voltage will tend to rise in absolute value as the luminance level is increased or the operating temperature is reduced.

Mode 2, selected by setting VCOMMODE=1h, is a hybrid control mode that prevents the absolute value of the cathode supply from becoming too small at higher temperatures, but allows it to increase at low temperatures where it is needed to ensure a stable regulated OLED current. Both the AUTO and MANUAL control loops are running simultaneously in this mode with one taking charge above a user defined threshold (set by register VCOM) and the other below that threshold. For relatively low temperatures and high luminance levels the AUTO mode will be in control and the cathode supply will follow the trajectory shown in Figure 20. If operating conditions try to force the absolute value of the cathode supply to drop below the threshold, then the control switches to MANUAL mode and the regulated supply remains fixed at the VCOM level.

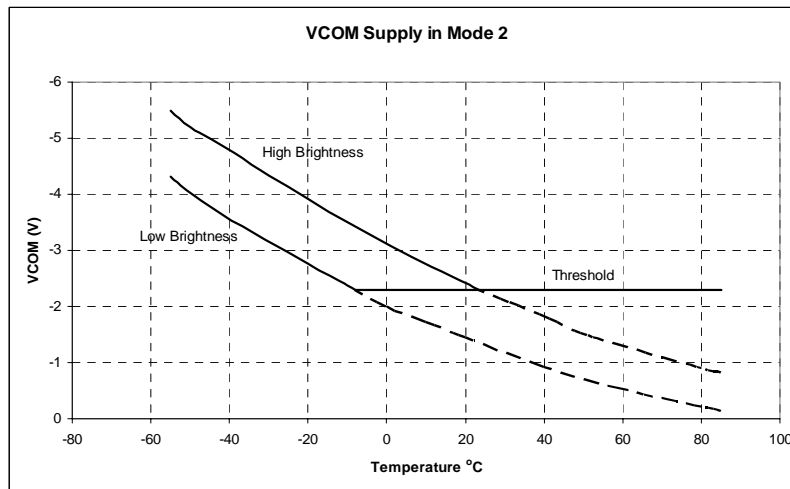


Figure 20 : VCOM supply characteristic in Mode 2

Mode 3, selected by setting VCOMMODE=2h, activates the Manual Loop which provides a fixed cathode supply based on a cathode voltage feedback signal. The actual value of the cathode voltage is controlled over a range of 0 to -6V by setting register VCOM. Its default value is about -2.3V. In this mode the dimming and luminance regulation functions via IDRFB and DIMCTL are not operational. Luminance is controlled directly via the VCOM register setting in this mode instead.

9.6 I²C Serial Interface

The serial interface consists of a serial controller and registers. The serial controller follows the I²C protocol. An active SCLK is required for the I²C interface to be operational. An internal address decoder transfers the content of the data into appropriate registers. The protocol will follow the address byte followed by register address data byte and register data byte sequence (3 bytes for each register access):

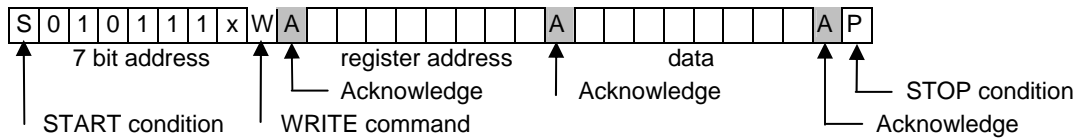
- Serial address with write command
- Register address
- Register data

The registers are designed to be read/write. Read mode is accomplished via a 4 byte sequence:

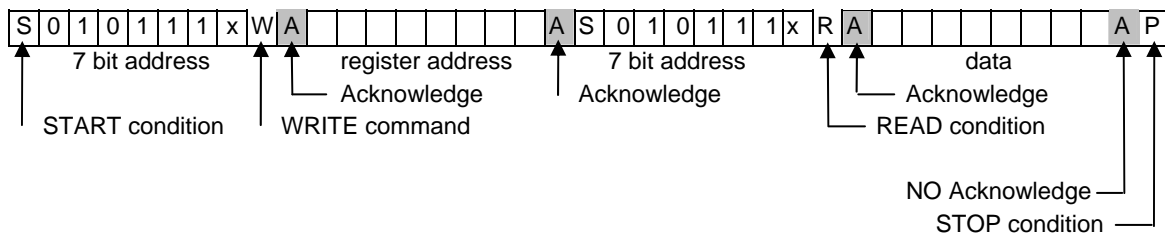
- Serial address with write command

Register address
Serial address with read command
Register data

RANDOM REGISTER WRITE PROCEDURE



RANDOM REGISTER READ PROCEDURE



The serial controller is capable of slave mode only.

The x in the 7-bit address code is set by the SERADD input pin and is provided to allow a dual display and single controller configuration.

Slave Address: 010111X where X = 0 or 1 depending on the status of the SERADD pin. This is summarized in Table 9-3.

Write Mode: Address is 5C (or 5E if SERADD = 1)

Read Mode: Address is 5D (or 5F is SERADD =1)

Sequential Read/Write Operation:

The serial controller allows for both sequential and read operational modes. For either mode, the host needs only set the initial register address followed by as many data bytes as needed, taking care not to issue a STOP condition until all desired data bytes have been transmitted (or received).

Maximum interface frequency: 400 KHz.

Table 9-3 : I²C Address Summary

SXGA		0	1	0	1	1	1	SA	w/r	
SA = 0	write:	0	1	0	1	1	1	0	0	= 0x 5C
	read:	0	1	0	1	1	1	0	1	= 0x 5D
SA = 1	write:	0	1	0	1	1	1	1	0	= 0x 5E
	read:	0	1	0	1	1	1	1	1	= 0x 5F

Note: When the RESETB pin is active (pulled low), the SXGA chip will pull the SDA pin low.

9.7 Power-On Sequence

To ensure proper startup and stabilization of the display the power-on sequence shown in the timing diagram of Figure 21 is recommended.

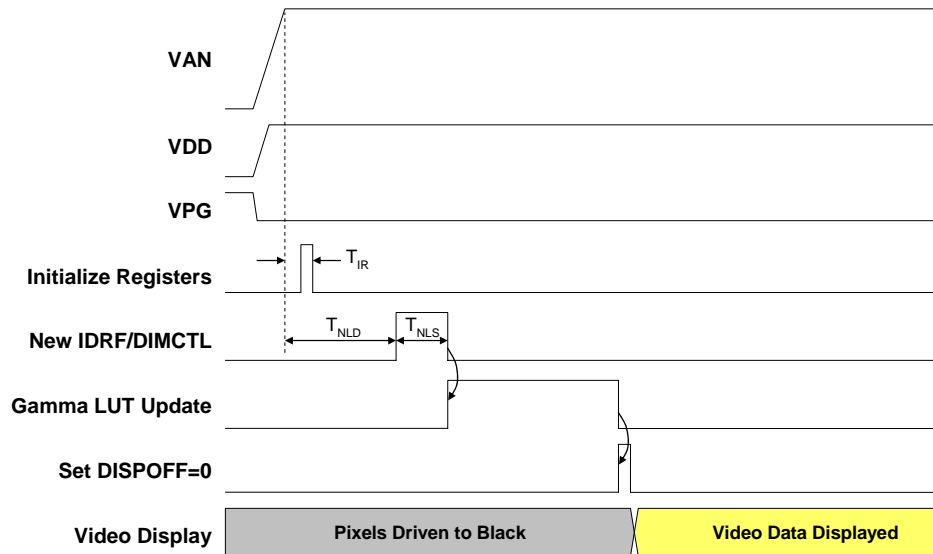


Figure 21 : Power-On sequence for supplies and control.

NOTE: Do not apply VAN without a VDD supply first. This will result in high current and possible device damage!

The key steps in the startup procedure are described below:

1. Turn on VDD, VAN, and VPG supplies – these can be simultaneous however the VDD supply should stabilize before the VAN supply reaches its turn-on threshold. A ramp-up time of 0.05 to 10ms for VAN and VDD is recommended for best performance. The turn-on time for VPG is not critical and it can be switched on anytime before the video data to the display is enabled.
2. An active SCLK should be connected to the SXGA display IC and pin RESETB tied high
3. Initialize the display registers – writing the values of register settings for the startup state of the display should be completed within the time interval T_{IR} . Normally these will comprise the last known operating state of the display except for the luminance settings. During initialization it is important to set IDRFB = 00h, DIMCTL = 01h, ANATEST = 44h, and leave register DISPOFF = 1 (display is off by default).

4. Set the startup luminance level – after a time delay T_{NLD} the startup (or last known luminance level) can be set by incrementing registers IDRFB and/or DIMCTL in steps of 1h via a sequence of serial port commands until the desired startup values are reached.
5. Update the gamma look-up-table (LUT) – the gamma for the display can be set after step 4 is completed. Using either a preset table or the auto-gamma feature described in section 9.4.5 the values for the gamma look-up-table are generated and uploaded to the external FPGA driver.
6. Turn on the display – after completion of step 5 the video data to the array is enabled by setting the DISPOFF bit in register DISPMODE to “0”. Prior to enabling video data the pixels in the array are actively driven to the black state.

Table 9-4: Power-On Timing Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Time from VAN threshold to end of register initialization	T_{IR}			30	ms
Time from VAN threshold to start of luminance register setting	T_{NLD}	100			ms

The currents supplied during a typical startup operation are illustrated in Figure 22. An inrush current (1) occurs on the 5V supply line during the initial moments of the ramp up phase (this is about 1A peak for a 100usec ramp time). Typically, using the startup procedure illustrated in Figure 21 the image will become active about 250msecs after power is applied. The current drawn from the 5V supply during normal operation (2) depends on the operating luminance.

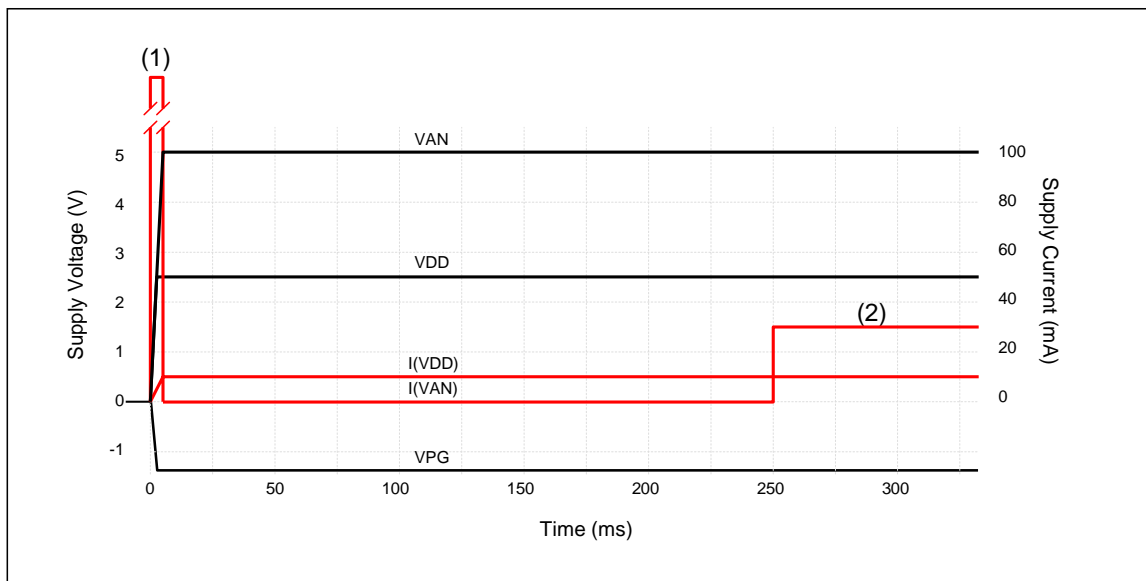


Figure 22: Typical startup currents

9.8 Power-Savings Mode

The display provides power down modes to minimize power consumption. This can occur in two ways:

- Sleep mode – manually controlled via the PDWN bit in register PWRDN, the entire display chip is powered down except for the serial interface. The register settings are saved and restored on power up from this mode.
- Individual block control – several functional blocks have the option to be turned off manually via control of register PWRDN.

The normal power-down sequence for supplies and control is given in Figure 23, while the power-down/power-on sequence for the sleep mode is shown in Figure 24. The data, sync and clock inputs should be inactive and held low to achieve the minimum sleep-mode power consumption.

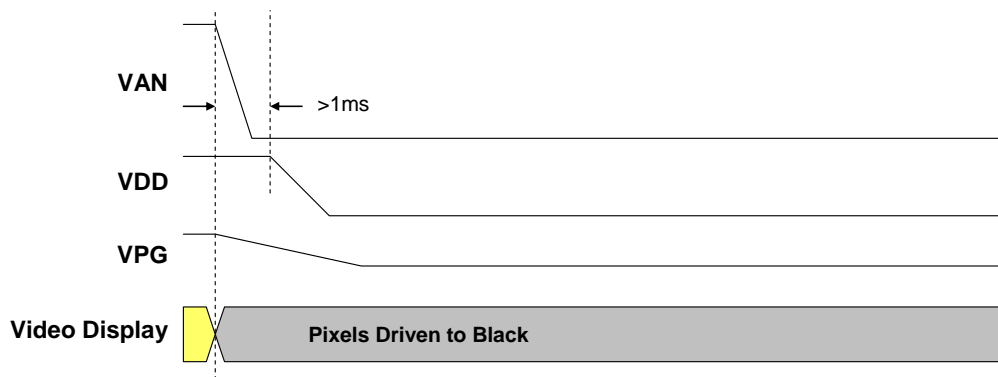


Figure 23: Power-Down sequence for supplies and control.

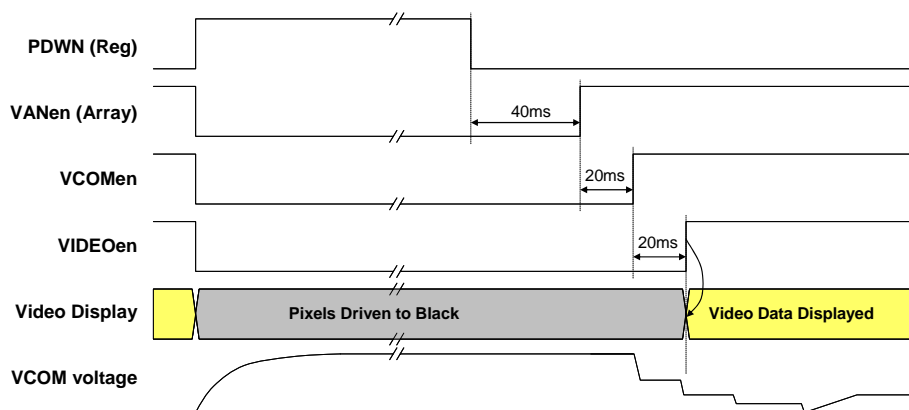


Figure 24 : Soft power-down / power-on sequence for supplies and control.

9.8.1 Display-Off Function

On power-up the microdisplay sets all internal registers to their default values and holds the array in the off state (black) until a software reset is externally applied. The DISPOFF bit in the DISPMODE register must be set to zero via the serial port in order for the array to become active.

10. REGISTER MAP SUMMARY

I2C Slave Address : 0101 11x

Cassini Register Map V2.3

Address (Hex)	Name	Access	Bit Name	Bit #	Reset Value (Hex)	Description	
00	STAT	R	REV	2-0	0	Silicon Revision Number	
Global Setting	01	VINMODE	R/W	SRESET	5	0	Software Reset. Clear all registers to default setting and hold until released. 0 = Released, 1 = Software Reset
				EXTRAMP	4	0	Select external RAMP 0 = use internal RAMP generator, 1 = use external RAMP input
				SET_ENABLE	3	0	ENABLE Active Level 0 = ENABLE active low, 1 = ENABLE active high
				SET_FIELD	2	0	FIELD Polarity 0 = Odd Field when ENABLE=Active, 1 = Even Field when ENABLE=Active
				VSYNCPOL	1	1	VSYNC Polarity 0 = Negative Sync, 1 = Positive Sync
				HSYNCPOL	0	1	HSYNC Polarity 0 = Negative Sync, 1 = Positive Sync
	02	DISPMODE	R/W	DISPOFF	5	1	Display Off (BURNIN mode override to ON) 0 = Display On, 1 = Display Off
				3D-MODE	4	0	3D Display Mode 0 = Normal Display, 1 = Time Sequential Mode
				RESOLUTION	3	0	Display Resolution 0 = SXGA/HD720, 1=DVGA (line & pixel doubling active)
				SCMODE	2	0	Progressive or Interlaced scan mode select 0 = Progressive, 1 = Interlaced
				VSCAN	1	0	Vertical Scan Direction 0 = Top to Bottom Scan, 1 = Bottom to Top Scan
				HSCAN	0	0	Horizontal Scan Direction 0 = Left to Right Scan, 1 = Right to Left Scan
	03	TOPPOS	R/W		7-0	06	Row Display Top Position (SXGA=06h, VGA=26h, 170M=26h, 720P=9Eh)
	04	BOTPOS	R/W		7-0	06	Row Display Bottom Position (SXGA=06h, VGA=26h, 170M=26h, 720P=9Eh)
DAC and RAMP Control	05	RAMPCTL	R/W	EXTRSEL	7	0	External resistor select 0 = Internal resistor select, 1 = External resistor select
				FLYBTIME	6	0	Ramp Fly back Time 0 = 500 nSec, 1 = 800 nSec
				RAMPDLY2	5-4	1	Ramp Delay by DCLK 00 = -1/2 DCLK, 01 = No Delay, 10 = +1/2 DCLK
				RAMPDLY1	3-0	0	Ramp Delay Fine Tune
	06	RAMPCM	R/W	RAMPDMON	7	0	Internal Ramp DAC Monitor Enable
				RAMPDCM	6-4	4	Ramp DAC Current Control (000 = -100%(Power down), 001 = -75%, 010 = -50%, 011 = -25%, 100 = ±0%, 101 = +25%, 110 = +50%, 111 = +75%)
				RAMPBMON	3	0	Internal Ramp Buffer Monitor Enable
				RAMPBCM	2-0	4	Ramp Buffer Current Control (000 = -100%(Power down), 001 = -75%, 010 = -50%, 011 = -25%, 100 = ±0%, 101 = +25%, 110 = +50%, 111 = +75%)
	07	DAOFFSET	R/W	DAOFFSETH	7-4	0	Ramp DAC Max Value Control, Up to +20 %
				DAOFFSETL	3-0	0	Ramp DAC Max Value Control, Down to -20 %
	08	EXTRAMPCTL	R/W	IRAMPHIGH	6	0	Internal Ramp DAC set All High (Active High)
				EXRAMPST	5-0	20	External RAMP start point set (16 SCLK to 48 SCLK after HSYNC rising edge) 10=16 SCLK, 11=17 SCLK, ...,20=32 SCLK, ...,30=48 SCLK
09	PWSAVE	R/W	RAMPPS	1	0	Ramp Buff Power Save Mode (RAMP Buffer ON only active video period) 0 = Normal Mode, 1 = Power Save Mode	
			GCPS	0	0	Global Counter Power Save Mode 0 = Disable (full 10bit Count), 1 = Enable (8bit & 10bit Count Combo)	
Sensors & Temp Control	0A	BIASN	R/W	BIASN	1-0	1	00 = bias current off 01 = bias current set to 0.5nA 10 = bias current set to 1nA
	0B	GAMMASET	R/W	VGNSEL	3	0	VGN Output select 0 = Full VGN output, 1 = VGN/2 output
				IDSTEP	2-0	0	Current level for gamma sensor
	0C	VCOMMODE	R/W		1-0	0	00 = AUTO1 mode 01 = AUTO2 mode 10 = MANUAL mode
	0D	VGMAX	R/W		7-0	0D	Fine adjustment for VGMAX level (default = 4.95V)
	0E	VCOM	R/W		7-0	51	VCOM manual setting (used when VCOMMODE = 01 or 10, default = -2.3V)
	0F	IDRF	R/W	IDRF_COARSE	7-5	1	Coarse adjustment for array reference current
				IDRF_FINE	4-0	10	Fine adjustment for array reference current
	10	DIMCTL	R/W		6-0	64	Dimming level control (default = 1X IDRF)
	11	TREFDIV	R/W		5-0	1E	Temp. Sensor Reference Clock Divider
	12	TEMPOFF	R/W		7-0	88	Temp. Sensor Offset
13	TUPDATE	R/W		7-0	FF	Number of frames per TEMPOUT update (Data range 02H - FFH) Update Time = (TUPDATE+1) * PERIOD _{FRAME} PERIOD _{FRAME} = 16.6 mSec when using 60Hz Video	
14	TEMPOUT	RO		7-0	-	Temperature Sensor Readout	
Power Down Control	15	PWRDN	R/W	PDWN	7	0	All system power down
				RDACPD	6	0	Ramp DAC power down
				BIASGENPD	5	0	BIASGEN power down
				TRAMPDP	4	0	Top Ramp Buffer power down
				BRAMPDP	3	0	Bottom Ramp Buffer power down
				VCMBP	2	0	VCOM generator bypass and power down
				TSENPDP	1	0	Temperature sensor power Down
				I2CPD	0	0	I2C power down (I2C setting freeze and can't change)

Test & Burn-In	16	TPMODE	R/W		2-0	0	Select test pattern for Built-In-Test-Mode (BI pin = 'High') x00= Burn-in (all white), x01=16 level gray scale, x10=Checkerboard 011= Alternating columns, 111 = Alternating rows.
					7	0	Reserved
	17	ANATEST	R/W		6	0	VTN monitor (ANA_TEST2 pin)
					5-3	0	Reserved
					2	0	VGMAX monitor (ANA_TEST1 pin)
					1-0	0	Reserved

11. DETAILED REGISTER DESCRIPTIONS

11.1 STAT (00h)

Name	STAT
Address	00h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
REV	2-0	0	Silicon revision number; Rev. 1 = 0

This register indicates the revision number of the silicon backplane design, with 0 corresponding to the first silicon known as Rev. 1.

11.2 VINMODE (01h)

Name	VINMODE
Address	01h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
SRESET	5	0	Software reset
EXTRAMP	4	0	RAMP source
SET_ENABLE	3	0	ENABLE active level
SET_FIELD	2	0	Field polarity
VSYNCPOL	1	1	VSYNC polarity
HYSYNCPOL	0	1	HSYNC polarity

SRESET:

- 1 = all internal registers are reinitialized to their default values and held there
- 0 = releases all internal registers from default state so they can be updated externally via I²C (default)

EXTRAMP:

- 1 = use external RAMP input (do not use)
- 0 = use internal RAMP input (default)

The RAMP is used for the digital-to-analog video data conversion. The external RAMP input option was included for test purposes and is not recommended for user application.

SET_ENABLE:

- 0 = the active state of the ENABLE input is set “low” (default)
- 1 = the active state of the ENABLE input is set “high”

The ENABLE input pin is used to implement 3D video modes using a single RGB source, with two consecutive frames carrying information for each eye. The microdisplay can be programmed for either an active high or low ENABLE input using the SET_ENABLE bit, allowing a single video signal to be used with two displays. In such a configuration, one display scans and displays, while the other one holds and displays. The active state of the ENABLE input corresponds to the video data being scanned and displayed by the microdisplay.

To implement the Frame Sequential 3D Mode according to the VESA Standard for Stereoscopic Display Hardware, the display for the left eye is programmed with SET_ENABLE=1 and the right eye display is programmed with SET_ENABLE=0. Consequently, the data for the left eye is supplied and displayed when ENABLE=1 while the display for the right eye displays the previous frame of data.

The ENABLE input pin is also used to indicate field polarity in non-3D interlaced modes. In this mode the SET_FIELD bit determines the field polarity when ENABLE is active.

SET_FIELD:

- 0 = Odd Field when ENABLE=Active (default)
- 1 = Even Field when ENABLE=Active

The SET_FIELD register determines the field polarity of the video signal when the ENABLE pin is active.

VSYNCPOL:

- 0 = Negative Sync
- 1 = Positive Sync (default)

HSYNCPOL:

- 0 = Negative Sync
- 1 = Positive Sync (default)

The SYNCPOL registers are used to determine whether the positive or negative edge of the external synchronization clocks (HSYNC and VSYNC) is used as the active transition by the internal display sequencers and control logic.

11.3 DISPMODE (02h)

Name	DISPMODE
Address	02h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
DISPOFF	5	1	Display On/Off control
3D-MODE	4	0	3D Mode control
RESOLUTION	3	0	Display resolution selection

SCMODE	2	0	Progressive or Interlaced scan mode selection
VSCAN	1	0	Vertical Scan direction
HSCAN	0	0	Horizontal Scan direction

DISPOFF:

- 0 = Display is turned ON
- 1 = Display is turned OFF (default)

The display starts in the OFF state by default and requires a command via the serial port to be turned on.

3D-MODE:

- 0 = Normal display mode (default)
- 1 = Time Sequential 3D mode

These bits are used to set the 3D mode of operation in conjunction with SET_ENABLE (bit #3 of the VINMODE register) and the Enable input. In Frame Sequential Mode each video frame contains information for either the left or right eye. When 3D-MODE="1" the SCSMODE bit in the DISPMODE register is overridden to Progressive Scan Mode (0h). The following description for Frame Sequential operation assumes the source is in compliance with the VESA standard, where the data for the left eye is provided while the Enable signal is at the logic high level, and the data for the right eye display is provided while the Enable signal is at the logic low level. The Enable input signal is sampled into the circuit by a flip-flop clocked on the falling edge of VSYNC and the sampled value is used for the next frame. (The Enable signal is generated by the graphics software and may not be synchronized to the VSYNC signal).

To activate the stereovision mode, the right eye display needs to be configured with Enable active low (SET_ENABLE= "0", bit #3 of the VINMODE register). This will allow the right eye microdisplay to hold the previous frame while the Enable input is high. The left eye display needs to be configured with Enable active high (SET_ENABLE="1", bit #3 of the VINMODE register). Thus the two Enable inputs can be tied together to the incoming Stereo Sync signal provided by the graphics adapter (or other custom source).

RESOLUTION:

- 0 = SXGA / HD720 resolution (default) and all other non-DVGA custom modes
- 1 = DVGA resolution (line and pixel doubling active)

SCSMODE:

- 0 = Progressive scan mode (default)
- 1 = Interlaced scan mode

Interlaced modes are limited to a maximum of 512 and a minimum of 240 active rows per field.

VSCAN:

- 0 = Top to Bottom vertical scan direction (default)
- 1 = Bottom to Top vertical scan direction

HSCAN:

- 0 = Left to Right horizontal scan direction (default)
- 1 = Right to Left horizontal scan direction

11.4 TOPPOS (03h)

Name	TOPPOS
Address	03h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	06	Top position of first active row

This register, along with register BOTPOS, is used to set the vertical position of the active display window within the 1036 available rows of pixels. In SXGA mode the active window can be moved by ± 6 lines from the center (default) position. Decreasing TOPPOS will shift the active window upwards in the display window. When TOPPOS is decreased, register BOTPOS must be increased by the same value so that the sum of the two remains equal. See BOTPOS for some typical settings.

11.5 BOTPOS (04h)

Name	BOTPOS
Address	04h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	06	Bottom position of last active row

This register, along with register TOPPOS, is used to set the vertical position of the active display window within the 1036 available rows of pixels. In SXGA mode the active window can be moved by ± 6 lines from the center (default) position. In HD720 mode the active window can be moved by a maximum of ± 255 lines from the center position. In DVGA mode the active window can be moved by ± 38 lines from the center position. Increasing BOTPOS will shift the active window upwards in the display window. When BOTPOS is increased, register TOPPOS must be decreased by the same value so that the sum of the two remains equal. Typical settings are given in the following table:

Vertical Position	Register	SXGA	DVGA	720P
Top	TOPPOS	00	00	3D
	BOTPOS	0C	4C	FF
Center	TOPPOS	06	26	9E
	BOTPOS	06	26	9E
Bottom	TOPPOS	0C	4C	FF
	BOTPOS	00	00	3D

11.6 RAMPCTL (05h)

Name	RAMPCTL
Address	05h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
EXTRSEL	7	0	NA
FLYBTIME	6	0	RAMP Flyback time
RAMPDLY2	5-4	1	RAMP delay in DCLK cycles
RAMPDLY1	3-0	0	RAMP delay fine tune

EXTRSEL:

- 0 = Internal resistor (default)
- 1 = External resistor

The EXTRSEL resistor option is not available for user application. Use only the default setting.

FLYBTIME:

- 0 = 500 ns (default)
- 1 = 800 ns

The FLYBTIME register is used to set the fly-back time for the internal RAMP.

RAMPDLY2:

- 00 = - 1/2 DLCK
- 01 = no delay (default)
- 10 = + 1/2 DCLK

The RAMPDLY2 register is used to adjust the starting position of the internal RAMP.

RAMPDLY1:

RAMPDLY1	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Delay time (ns)	0	0.62	1.13	1.69	2.20	2.72	3.24	3.76	4.24	4.86	5.37	5.93	6.44	6.96	7.48	8.0

The RAMPDLY1 register is used to fine tune the starting position of the internal RAMP.

11.7 RAMPCM (06h)

Name	RAMPCM
Address	06h
Mode	Read / Write

Bit Name	Bit#	Reset	Description
----------	------	-------	-------------

		Value	
RAMPDMON	7	0	Internal RAMP DAC monitor enable
RAMPDCM	6-4	4	RAMP DAC current control
RAMPBMON	3	0	Internal RAMP buffer monitor enable
RAMPBCM	2-0	4	RAMP buffer current control

RAMPDMON:

- 0 = Disable internal RAMP DAC monitoring (default)
- 1 = Enable internal RAMP DAC monitoring

The RAMPDMON register is used to enable monitoring of the internal RAMP DAC signal.

Note: DO NOT enable this register as the RAMP pin is grounded on the R1 carrier board.

RAMPDCM:

- 000 = -100% (power down)
- 001 = -75%
- 010 = -50%
- 011 = -25%
- 100 = nominal (default)
- 101 = +25%
- 110 = +50%
- 111 = +75%

The RAMPDCM register is used to set the operating bias current for the internal RAMP DAC. The settings reduce or increase the current by a percentage of the nominal (default) value.

RAMPBMON:

- 0 = Disable internal RAMP buffer monitoring (default)
- 1 = Enable internal RAMP buffer monitoring

The RAMPBMON register is used to enable testing of the internal RAMP buffer signal. This function is only available on units specifically packaged for testing and is not accessible to the user.

RAMPBCM:

- 000 = -100% (power down)
- 001 = -75%
- 010 = -50%
- 011 = -25%
- 100 = nominal (default)
- 101 = +25%
- 110 = +50%
- 111 = +75%

The RAMPBCM register is used to set the operating bias current for the internal RAMP DAC buffer amplifier. The settings reduce or increase the current by a percentage of the nominal (default) value.

11.8 DAOFFSET (07h)

Name	DAOFFSET
Address	07h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
DAOFFSETH	7-4	0	RAMP DAC maximum value increase control
DAOFFSETL	3-0	0	RAMP DAC maximum value decrease control

DAOFFSETH:

0h = no change (default)
Fh = +20% change

DAOFFSETL:

0h = no change (default)
Fh = -20% change

Registers DAOFFSETH and DAOFFSETL are used to adjust the maximum value of the internal RAMP DAC signal. DAOFFSETH can increase the maximum level by up to +20% and DAOFFSETL can decrease the maximum level by up to -20% of the nominal value.

The typical dependence of display luminance on DAOFFSET(d) is shown in Figure 25. The luminance is seen to saturate for DAOFFSET greater than 4 in this sample. For normal operation DAOFFSET should be set to about 88% of the saturation value as shown in the figure.

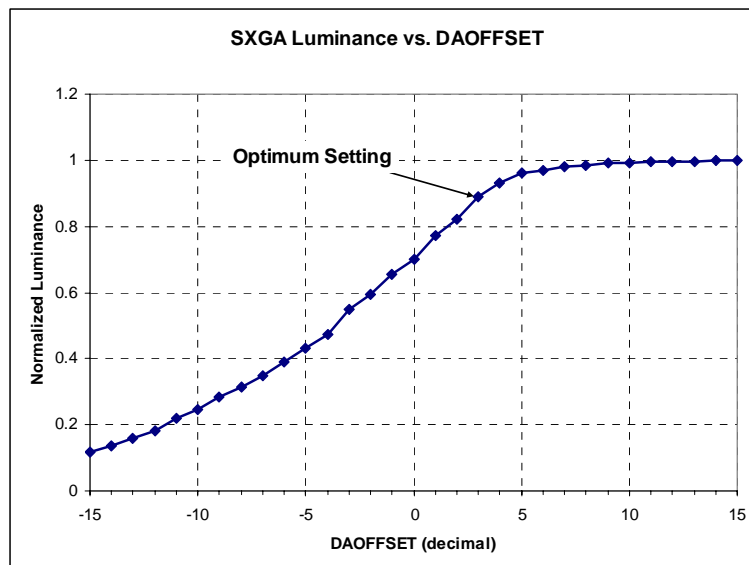


Figure 25: Luminance dependency on DAOFFSET

11.9 EXTRAMPCTL (08h)

Name	EXTRAMPCTL
Address	08h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
IRAMPHIGH	6	0	Set internal RAMP DAC to high level
EXTRAMPST	5-0	20	NA

IRAMPHIGH:

- 0 = normal operation (default)
- 1 = internal RAMP DAC is set to fixed maximum level

The IRAMPHIGH register is used to set the start point of the internal RAMP DAC to its maximum value and keep it there until the register is reset.

EXTRAMPST:

This option is not available for user application.

11.10 PWSAVE (09h)

Name	PWSAVE
Address	09h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
RAMPPS	1	0	RAMP buffer power saving mode
GCPS	0	0	Global counter power saving mode

RAMPPS:

- 0 = RAMP buffer power saving mode off (default)
- 1 = RAMP buffer power saving mode on

The RAMPPS register is used to enable the RAMP DAC buffer power saving option in which the buffer is only switched on during active video periods.

GCPS:

- 0 = Global Counter power saving mode off (default)
- 1 = Global Counter power saving mode on

The GCPS register is used to enable the Global Counter power saving option in which the internal D/A converter operates in a hybrid 8-bit/10-bit conversion mode.

11.11 BIASN (0Ah)

Name	BIASN
Address	0Ah
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	1-0	1	Set pixel bias current

BIASN:

- 00 = pixel bias current is turned off
- 01 = pixel bias current set to 0.5nA (default)
- 10 = pixel bias current set to 1nA

The BIASN register is used to set the sink current applied in each pixel cell. It is recommended to use the BIASN=10 setting in normal operation for best performance.

11.12 GAMMASET (0Bh)

Name	GAMMASET
Address	0Bh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
VGNSEL	3	0	VGN output range setting
IDSTEP	2-0	0	Current level for gamma sensor

VGNSEL:

- 0 = Full VGN output range, 0 to VAN (default)
- 1 = VGN/2 output range, 0 to VAN/2

The VGNSEL register is used to select the VGN signal output range. It can be set to either 0 to VAN or 0 to VAN/2.

IDSTEP:

- 0h \approx IDR/128
- 1h \approx IDR/64
- 2h \approx IDR/32
- 3h \approx IDR/16
- 4h \approx IDR/8
- 5h \approx IDR/4

6h \approx IDRF/2
7h = IDRF

The IDSTEP register is used to set the current level for the gamma sensor. The corresponding output voltage is provided at pin VGN.

A minimum of 10msec following an IDSTEP register update should be allowed for the VGN signal to settle before sampling. In addition, sampling of the VGN signal should be carried out during the Frame Blanking time.

11.13 VCOMMODE (0Ch)

Name	VCOMMODE
Address	0Ch
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	1-0	0	Set internal VCOM supply mode

This register sets the operating mode of the internal VCOM dc-dc converter.

00 = AUTO1 mode (default)
01 = AUTO2 mode
10 = MANUAL mode

In the AUTO1 mode, the VCOM converter uses an internal current reference to maintain a fixed OLED current level, which is defined by registers DIMCTL and IDRF.

In the AUTO2 mode, the VCOM converter regulates the OLED current level when the VCOM supply is below a set threshold (defined by the VCOM register), and clamps the output to the threshold level when conditions call for a VCOM output above the threshold level.

In the Auto 3 mode, the VCOM converter uses a voltage reference signal to maintain a fixed cathode supply voltage. The value of the cathode voltage is set by register VCOM.

11.14 VGMAX (0Dh)

Name	VGMAX
Address	0Dh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0D	Fine adjustment for VGMAX level

00h = 5 (VAN = 5V)
0Dh = 4.95 (default)
FFh = 4

$$VGMAX \text{ level} = VAN * (1 - 0.2 * VGMAX(\text{dec}) / 255)$$

This register sets the pixel voltage at which the maximum OLED current is regulated. It should be slightly below the VAN supply to prevent saturation of the video buffer amplifiers.

11.15 VCOM (0Eh)

Name	VCOM
Address	0Eh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	51	VCOM manual setting

Cathode supply as a function of VCOM setting:

VCOM(h)	FF	F0	E0	D0	C0	B0	A0	90	80	70	60	51*	40	30
Voltage	-0.29	-0.38	-0.47	-0.59	-0.72	-0.85	-1.0	-1.2	-1.43	-1.7	-2.0	-2.4	-2.97	-3.68

*default value

Register VCOM[7,0] sets the fixed output level for the internal VCOM inverter when VCOMMODE =01 or 10. There is no compensation for the variation in OLED behavior with temperature in this mode of operation. As a result, a setting at room temperature will not necessarily result in optimal contrast and the same luminance at other temperatures. The default setting (51h) will result in a cathode supply \approx -2.3V. The typical dependency of luminance on the VCOM setting in manual mode is given in Figure 26 for a color display.

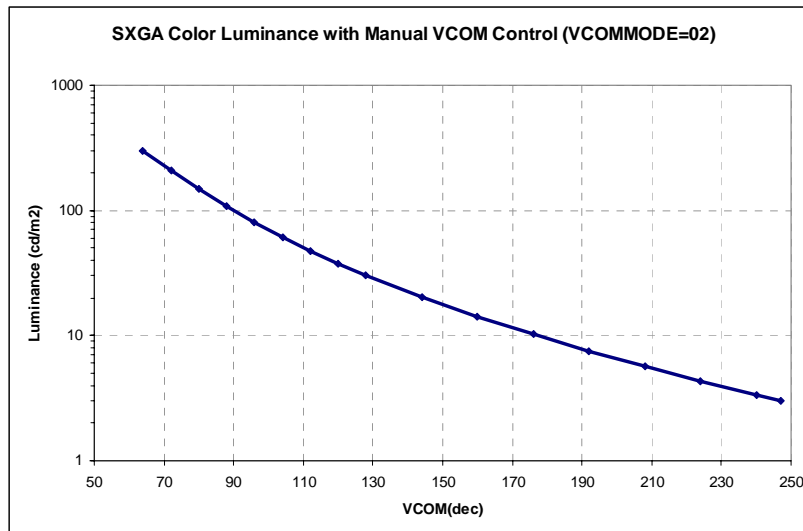


Figure 26: Typical luminance dependency on manual VCOM setting

11.16 IDRFB (0Fh)

Name	IDRF
Address	0Fh
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
IDRF_COARSE	7-5	1	Coarse adjustment for array reference current
IDRF_FINE	4-0	10	Fine adjustment for array reference current

IDRF_COARSE:

IC#
 0h = 0
 1h = 0.5 (default)
 2h = 1.5
 3h = 2.5
 4h = 3.5

IDRF_FINE:

IF#
 00h = 0
 01h = 1/32
 ...
 10h = 16/32 (default)
 ...
 1Fh = 31/32

Register IDRFB is used to set the maximum OLED current, which determines the luminance level for the display. The luminance will be directly proportional to the IDRFB factor (sum of IC# and IF#) and the reference luminance LDEF as given by the following expression:

$$LMAX = LDEF * (IC# + IF#) \quad \text{in cd/m}^2$$

where the white luminance for a color display is $LDEF \approx 75 \text{cd/m}^2$ at the default settings (see table below).

IDRF (hex)	LMAX / LDEF
0	0
10	0.5
20	0.5
30	1
40	1.5
50	2
60	2.5
70	3
80	3.5

Note: When increasing the luminance in the display via a serial interface command the step increase in the IDRFB register should be limited to no more than 1h per each I²C write sequence to avoid flicker.

11.17 DIMCTL (10h)

Name	DIMCTL
Address	10h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	6-0	64	Dimming level control

00h = 0
 01h = 1% of LMAX
 ...
 64h = 100% of LMAX
 ...
 7Fh = 127% of LMAX

This register provides linear control of the display luminance level ranging from 0 to 127% in steps of 1%. The default value of 64h is equal to 100% of the luminance defined by register IDRFB.

This register is only operational in Auto VCOM mode (VCOMMODE=00).

Note: When increasing the luminance in the display via a serial interface command the step increase in the DIMCTL register should be limited to no more than 1h per each I²C write sequence to avoid flicker.

11.18 TREFDIV (11h)

Name	TREFDIV
Address	11h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	5-0	1E	Temperature sensor reference clock divider adjust

The register TREFDIV is used to adjust the slope of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -40 to 80°C, although the setting is best determined by a calibration measurement of the display in its final assembly.

See the description for register TEMPOUT.

11.19 TEMPOFF (12h)

Name	TEMPOFF
Address	12h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	88	Temperature sensor offset adjust

The register TEMPOFF is used to adjust the offset of the temperature readout sensor, TEMPOUT, to correspond to the desired operating range of the display. The default setting is intended to support a full scale temperature range of -40 to 80°C, although the setting is best determined by a calibration measurement of the display in its final assembly.

See the description for register TEMPOUT.

11.20 TUPDATE (13h)

Name	TUPDATE
Address	13h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	FF	Number of frames per TEMPOUT update

This register sets the update rate of the Temperature Sensor reading, TEMPOUT. The time between sensor updates is given by:

$$\text{Update Time} = (\text{TUPDATE}(\text{decimal}) + 1) * T_{\text{FRAME}}$$

where the frame period T_{FRAME} is equal to 16.6 ms for 60Hz video. The valid range for TUPDATE is 02h to FFh.

11.21 TEMPOUT (14h)

Name	TEMPOUT
Address	14h
Mode	Read Only

Bit Name	Bit#	Reset Value	Description
	7-0	-	Temperature sensor readout

Register TEMPOUT provides an 8bit digital output that is linearly proportional to the chip temperature. The SXGA display temperature sensor is designed around a P-N junction. The output of the junction is sampled by an internal current to voltage converter, digitized and stored into a dedicated 8-bit register TEMPOUT. The sampling rate is controlled by configuration register TUPDATE (13H). By default the temperature sensor is updated once every 255 frames. Two registers are used to set the sensor gain (TREFDIV) and sensor offset (TEMPOFF). The temperature sensor can be powered down when not used by setting TSENPD =1 in the PWRDN register.

The temperature sensor is intended to provide a full-scale reading over a temperature range defined by the user. Assuming that the desired operating temperature range is defined by T_{MIN} and T_{MAX} , the expected sensor response would be as follows:

$$TEMPOUT(dec) = A * temp + B$$

where temp is the chip temperature in degrees Celsius, and A and B are given by:

$$A = \frac{255}{T_{MAX} - T_{MIN}}$$
$$B = \frac{-255 * T_{MIN}}{T_{MAX} - T_{MIN}}$$

The actual sensor response is determined by registers TREFDIV and TEMPOFF through the following relationship:

$$TEMPOUT(d) = k_1 * TREFDIV(d) * temp + k_2 + TEMPOFF(d)$$

The constants k_1 and k_2 are dependent on properties of the silicon and package assembly. For example, the average register settings needed to achieve a working temperature range of -60°C to +80°C are given by the following values for package A04-500463-01:

$$TREFDIV(d) = 25$$
$$TEMPOFF(d) = 93$$

Using these values will result in a variation in temperature reading from part to part due to manufacturing tolerances. To get a reasonably good sensor performance it is usually enough to just find the optimum value for TEMPOFF which requires only one measurement at room temperature. Increased accuracy can be obtained for a specific part by performing the calibration measurements described below.

To find the optimum value for TREFDIV do the following:

- Place the display in a temperature controlled environment, e.g. an oven
- Set TREFDIV=25d=19h and TEMPOFF=0
- Set DISPMODE=20h (turn off the display)
- Read TEMPOFF at several ambient temperatures, e.g. 0°C, 20°C, 40°C, 60°C
- Take the slope to find the sensor response, $A_{MEAS} = dTEMPOUT(d)/dtemp$
- The optimum value for TREFDIV is then given by

$$TREFDIV_{OPT} = 25 * \frac{1.82}{A_{MEAS}}$$

To find the optimum value for TEMPOFF do the following:

- Set TREFDIV=25d=19h (or the optimum value) and TEMPOFF=0
- Set DISPMODE=20h (turn off the display)
- Allow several minutes to stabilize and then read TEMPOUT_{AMB} and the ambient temperature T_{AMB}
- The optimum value for TEMPOFF is then given by

$$TEMPOFF_{OPT} = 1.82 * T_{AMB} + 109 - TEMPOUT_{AMB}$$

With these settings, the microdisplay temperature can be found from the sensor reading through the following relationship:

$$T(^{\circ}C) = \frac{140}{255} * TEMPOUT(d) - 60$$

Temperatures below -60°C will return a TEMPOUT reading of 0 and temperatures above +80°C will return a hexadecimal value of FF.

11.22 PWRDWN (15h)

Name	PWRDWN
Address	15h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
PDWN	7	0	All systems power down
RDACPD	6	0	RAMP DAC power down
BIASGENPD	5	0	BIASGEN power down
TRAMPPD	4	0	Top RAMP buffer amp power down
BRAMPPD	3	0	Bottom RAMP buffer amp power down
VCMBP	2	0	VCOM generator bypass and power down
TSENDP	1	0	Temperature sensor power down
I2CPD	0	0	I ² C power down

PDWN:

- 1 = all systems are powered down
- 0 = normal operation (default)

By setting the PDWN bit to a “1” the chip enters a deep sleep mode in which all functions including the I²C interface are powered down in order to minimize power consumption. The data, sync and clock inputs

should be inactive and held low to achieve the lowest power consumption. An on-chip Address Detection circuit monitors the I²C input lines and resets the PDWN bit when it detects the correct I²C address, restoring the display to operating mode.

All register settings are saved in the power down mode and the display will restart in its previous state when normal operation is resumed.

RDACPD:

- 1 = internal RAMP DAC is powered down (use when external RAMP option is enabled)
- 0 = internal RAMP DAC is operational (default)

The internal RAMP DAC generator may be power down if an external RAMP source is used.

BIASGENPD:

- 1 = Bias generator is powered down
- 0 = Bias generator is operating normally (default)

TRAMPPD:

- 1 = the top RAMP buffer amplifier is powered down
- 0 = the top RAMP buffer is operating normally (default)

BRAMPPD:

- 1 = the bottom RAMP buffer amplifier is powered down
- 0 = the bottom RAMP buffer is operating normally (default)

VCMBP:

- 1 = the dc-dc converter used to generate VCOM is bypassed and powered down
- 0 = the dc-dc converter is operating normally (default)

The internal VCOM generator may be deactivated if an external VCOM supply is used.

TSENDP:

- 1 = the Temperature Sensor is powered down
- 0 = the Temperature Sensor is operating normally (default)

The temperature sensor can be turned off by register TSENDP when a temperature readout is not needed.

I2CPD:

- 1 = the I²C serial port is powered down
- 0 = the I²C serial port is operating normally (default)

If the serial port is turned off the register settings are frozen and cannot be changed unless a power reset is carried out.

11.23 TPMODE (16h)

Name	TPMODE
Address	16h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	2-0	0	Select test pattern for Burn-In mode

The BI pin must be tied high to activate the Burn-In test mode which can be used to check display functionality without the presence of external video data or clock signals. In this mode the display generates data, syncs and the pixel clock internally for several different video patterns. The TPMODE register is used to select one of the built-in test patterns in Burn-In mode via the serial interface.

- 000 or 100 = all white pattern (default)
- 001 or 101 = 16 level gray scale pattern without gamma correction
- 010 or 110 = checkerboard pattern
- 011 = alternating columns pattern
- 111 = alternating rows pattern

11.24 ANATEST (17h)

Name	ANATEST
Address	17h
Mode	Read / Write

Bit Name	Bit#	Reset Value	Description
	7-0	0	Select test function

Note! This register should be set to 44h immediately on power-up and after any reset condition to allow proper operation of the display in Auto VCOM mode.

12. APPENDIX A: APPLICATION SYSTEM DIAGRAM

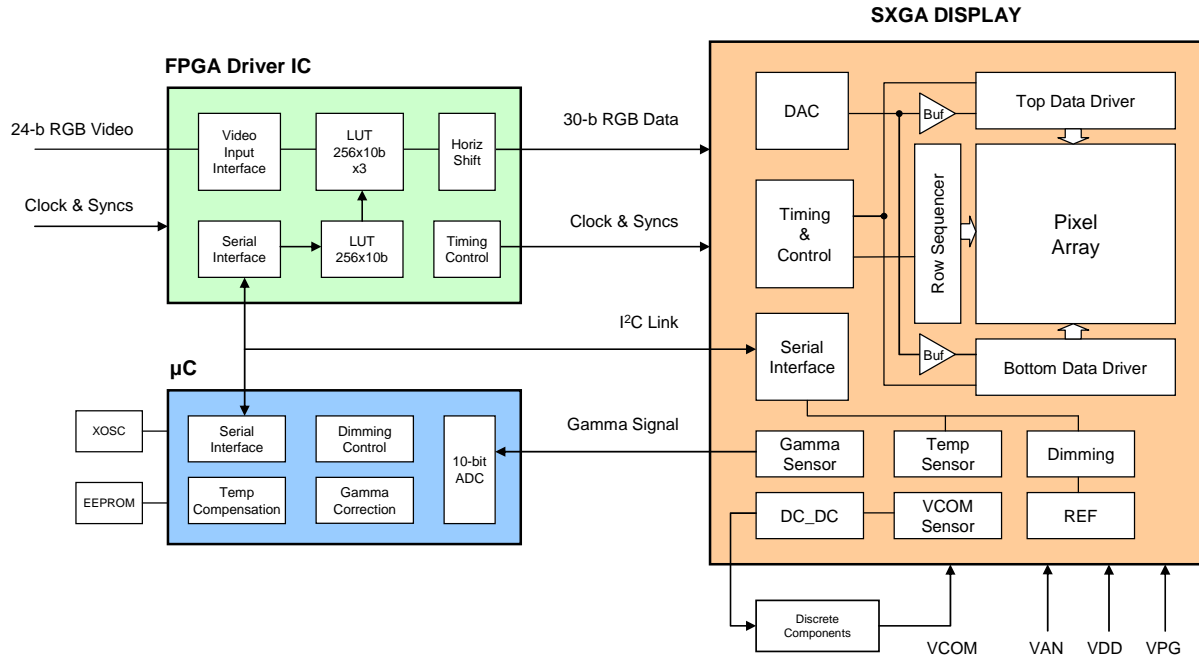


Figure 27 : Block diagram of application reference system

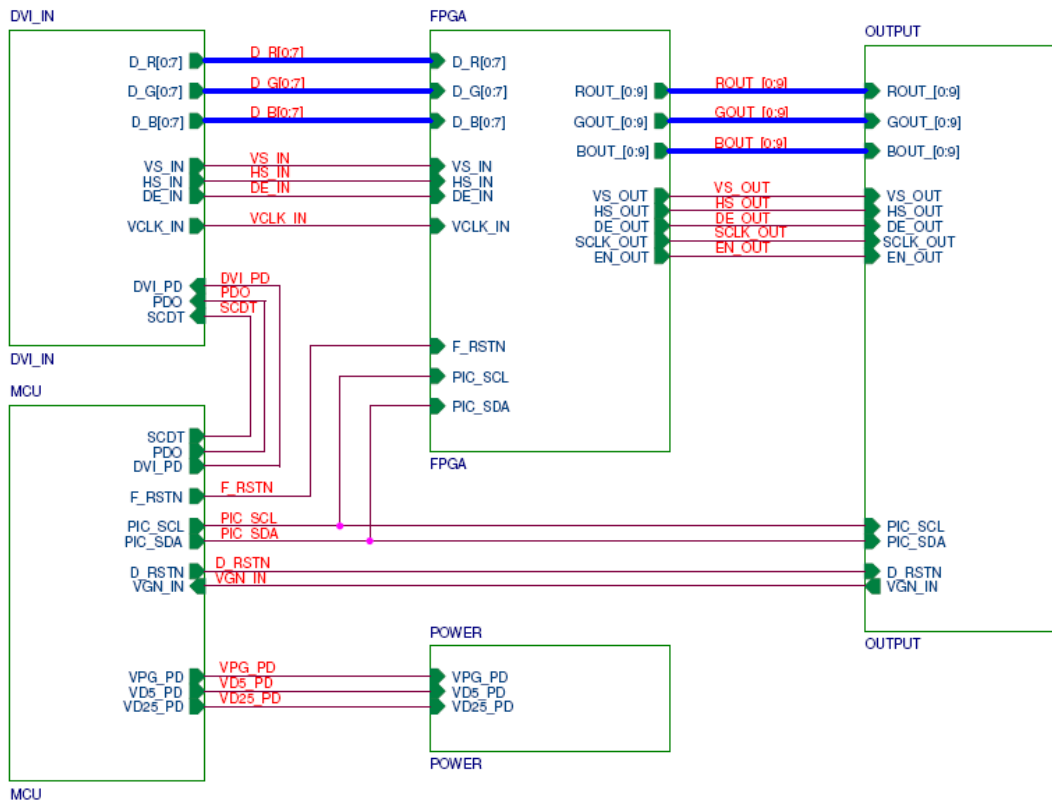


Figure 28 : Top-level schematic of development board (A01-500467-02)

13. APPENDIX B: MICRODISPLAY CARRIER BOARD

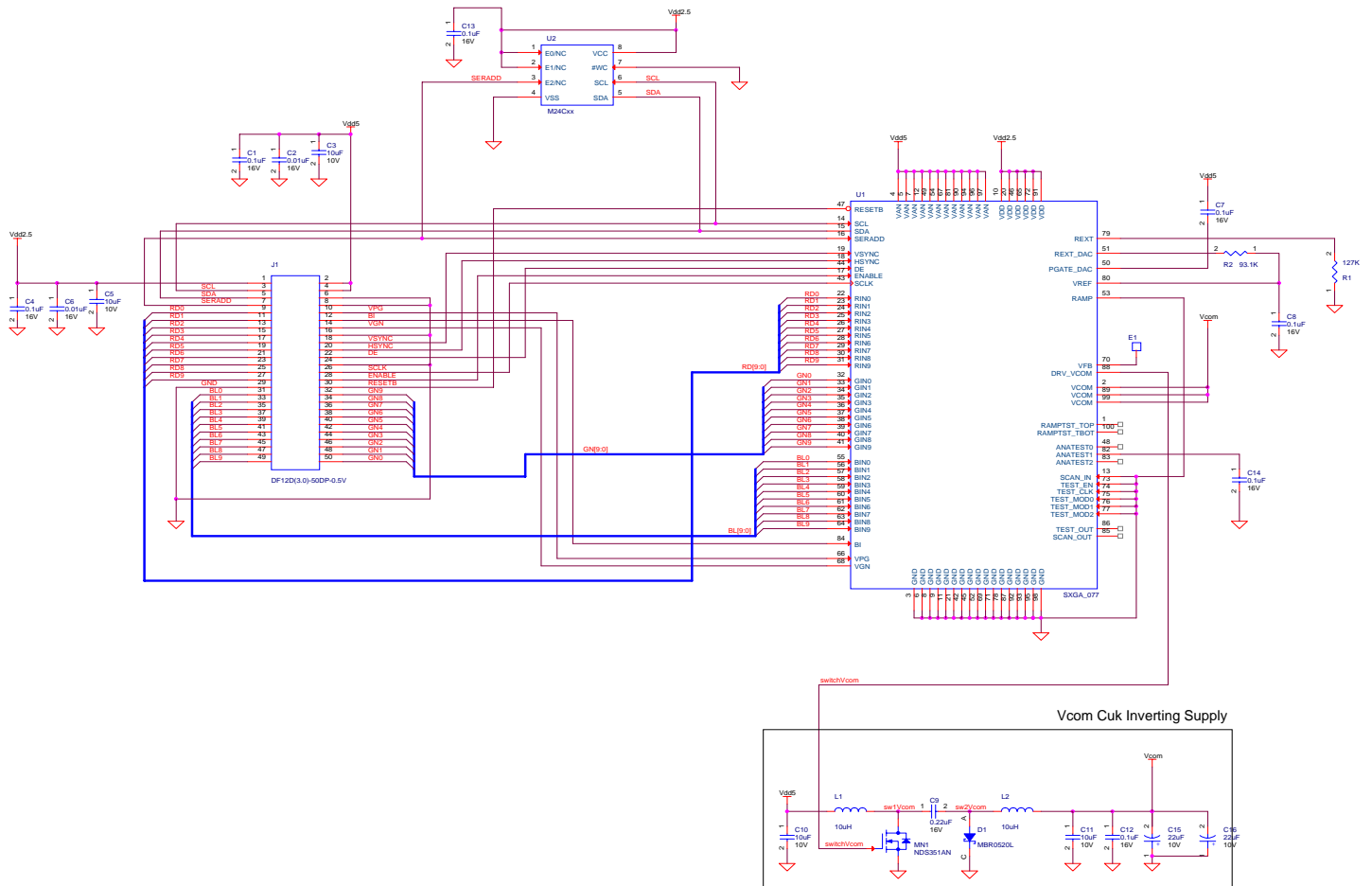


Figure 29 : Carrier board schematic (D01-500463-05)

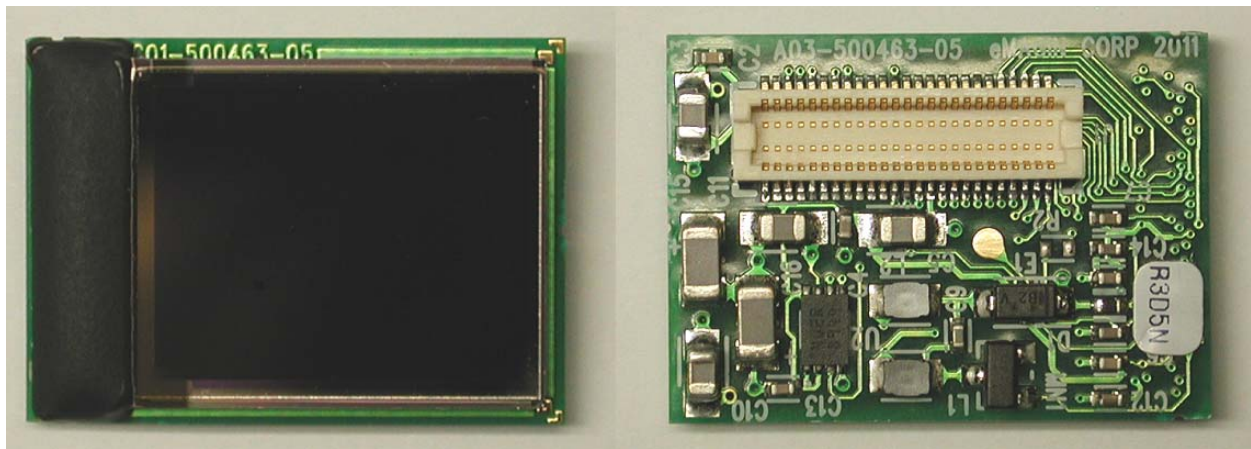


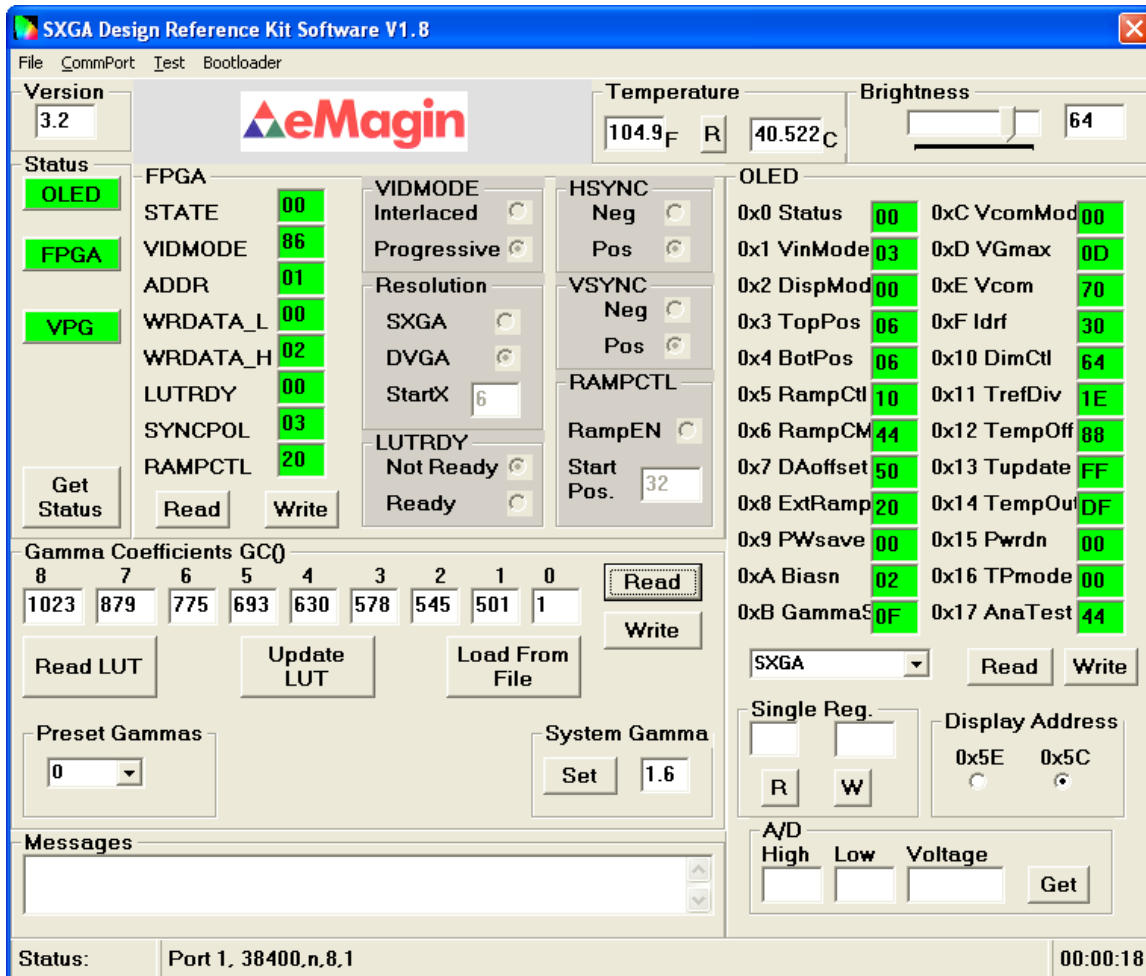
Figure 30: Photo of Microdisplay Assembly (A04-500463-05)

14. APPENDIX C: MICRODISPLAY ASSEMBLY BILL OF MATERIALS

Item #	Quantity	Reference	Description	Value	Mfg	Mfg Part #	RoHS Compliant
1	4	C3,C5,C10,C11	CAP,10uF,10V,10%,CER,X5R,0805	10uF	Taiyo Yuden	LMK212BJ106KG-T	Y
2	1	C9	CAP,0.22uF,16V,10%,CER,X5R,0402	0.22uF	Taiyo Yuden	EMK105BJ224KV-F	Y
3	7	C1,C4,C7,C8,C12,C13,C14	CAP,0.1uF,16V,10%,CER,X5R,0402	0.1uF	Murata	GRM155R61C104KA88D	Y
4	2	C2,C6	CAP,0.01uF,25V,10%,CER,X7R,0402	0.01uF	Panasonic	ECJ-0EB1E103K	Y
5	2	C15, C16	CAP CER 22UF 10V CER X5R 1206	22uF	Taiyo Yuden	LMK316BJ226ML-T	Y
6	1	D1	Diode,Schottky Barrier,20V,0.5A,SOD-123	MBR0520L	Fairchild Semiconductor	MBR0520L	Y
7	2	L1,L2	INDUCTOR 10UH 225MA 0806	10uH	Murata	LQH2MCN100K02L	Y
8	1	MN1	MOSFET,N-channel,30V,1.2A,SSOT23	NDS351AN	Fairchild Semiconductor	NDS351AN	Y
9	1	PCB1	PCB Fab	C01-500463-05	eMagin		Y
10	1	R1	Res,127K,.062W,1%,0402,100ppm	127K	Panasonic	ERJ-2RKF1273X	Y
11	1	J1	Con,50p,0.5mm,receptacle, Hirose, DF12D(3.0)-50DP-0.5V	DF12D(3.0)-50DP-0.5V	Hirose	DF12D(3.0)-50DP-0.5V	Y
13	1	U2	IC EEPROM 2KBIT 400KHZ 8UFDFPN	NA	ST Micro	M24C02-RMB6TG	Y
12	1	U1	OLED Microdisplay Die	DNI(SXGA_077 DIE REV3)	eMagin	A03-500672-00	Y
13	1	U2	IC EEPROM 2KBIT 400KHZ 8UFDFPN	NA	ST Micro	M24C02-RMB6TG	Y

15. APPENDIX D: TYPICAL REGISTER SETTING

Recommended Register Settings for Normal Operation



Notes:

1. Value of register DAoffset is specific to each individual device and should be calibrated
2. Registers TrefDiv and TempOff can be adjusted for best temperature reading accuracy
3. Register AnaTest (17h) must be set to 44h for operation with VcomMode=00

16. APPENDIX E: EEPROM MEMORY MAP

The SXGA microdisplays contains an EEPROM memory device to serve as non-volatile data storage for retrieving display specific information, such as its serial number and optimal registers values for proper operation. The data can be accessed via the same I²C serial interface that is used to communicate with the microdisplay. The device's serial address is as follows:

Write Mode: Address is A6h (or AEh if SERADD = 1) – *Prohibited mode*

Read Mode: Address is A7h (or AFh if SERADD =1)

The first 5 bytes represent unique serial number of the SXGA microdisplay. The next 24 bytes contain sequential data values that can be used to write to the microdisplay's internal registers starting with register address, "00h", to "17h". Then the following 10 bytes contain its process lot and wafer information.

NOTE: The EEPROM is not write-protected and care should be taken not to activate the Write Mode. The values highlighted in gray are measured at the factory and are specific to each individual device.

SXGA Microdisplay's Onboard EEPROM	
Address (hex)	Data Description
<i>00</i>	Serial Char #0
<i>01</i>	Serial Char #1
<i>02</i>	Serial Char #2
<i>03</i>	Serial Char #3
<i>04</i>	Serial Char #4
<i>05</i>	Data #0 / STAT
<i>06</i>	Data #1 / VINMODE
<i>07</i>	Data #2 / DISPMODE
<i>08</i>	Data #3 / TOPPOS
<i>09</i>	Data #4 / BOTPOS
<i>0A</i>	Data #5 / RAMPCTL
<i>0B</i>	Data #6 / RAMPCM
<i>0C</i>	Data #7 / DAOFFSET
<i>0D</i>	Data #8 / EXTRAMPCTL
<i>0E</i>	Data #9 / PWSAVE
<i>0F</i>	Data #10 / BIASN
<i>10</i>	Data #11 / GAMMASET
<i>11</i>	Data #12 / VCOMMOMODE

12	Data #13 / VGMAX
13	Data #14 / VCOM
14	Data #15 / IDRF
15	Data #16 / DIMCTL
16	Data #17 / TREFDIV
17	Data #18 / TEMPOFF
18	Data #19 / TUPDATE
19	Data #20 / TEMPOUT
1A	Data #21 / PWRDN
1B	Data #22 / TPMODE
1C	Data #23 / ANATEST
1D	Lot Char#0
1E	Lot Char#1
1F	Lot Char#2
20	Lot Char#3
21	Lot Char#4
22	Lot Char#5
23	Wafer Char#0
24	Wafer Char#1
25	Wafer Char#2
26	Wafer Char#3